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Nathan et al.

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(45) **Date of Patent: Feb. 19, 2013**

(54) **METHOD AND SYSTEM FOR PROGRAMMING AND DRIVING ACTIVE MATRIX LIGHT EMITTING DEVICE PIXEL HAVING A CONTROLLABLE SUPPLY VOLTAGE**

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(73) Assignee: **Ignis Innovation Inc.**, Waterloo (CA)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Sep. 23, 2011**

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Related U.S. Application Data

(63) Continuation of application No. 12/851,652, filed on Aug. 6, 2010, which is a continuation of application No. 11/298,240, filed on Dec. 7, 2005, now Pat. No. 7,800,565.

(30) **Foreign Application Priority Data**

Dec. 7, 2004 (CA) 2490858

(51) **Int. Cl.**
G09G 3/30 (2006.01)

(52) **U.S. Cl.** **345/78**; 345/82

(58) **Field of Classification Search** 345/76–78, 345/82–83; 315/169.3
See application file for complete search history.

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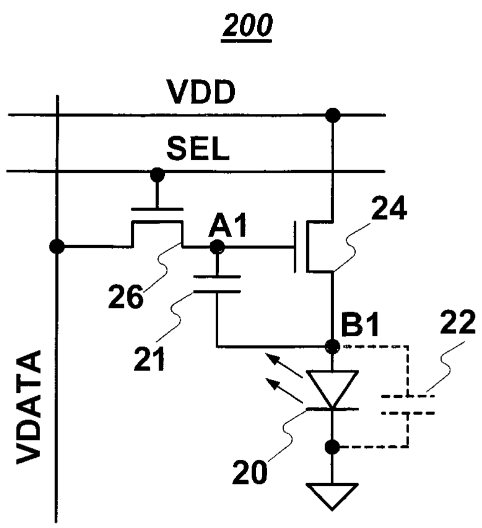
(57) **ABSTRACT**

Method and system for programming and driving active matrix light emitting device pixel is provided. The pixel is a voltage programmed pixel circuit, and has a light emitting device, a driving transistor and a storage capacitor. The pixel has a programming cycle having a plurality of operating cycles, and a driving cycle. During the programming cycle, the voltage of the connection between the OLED and the driving transistor is controlled so that the desired gate-source voltage of a driving transistor is stored in a storage capacitor.

18 Claims, 22 Drawing Sheets



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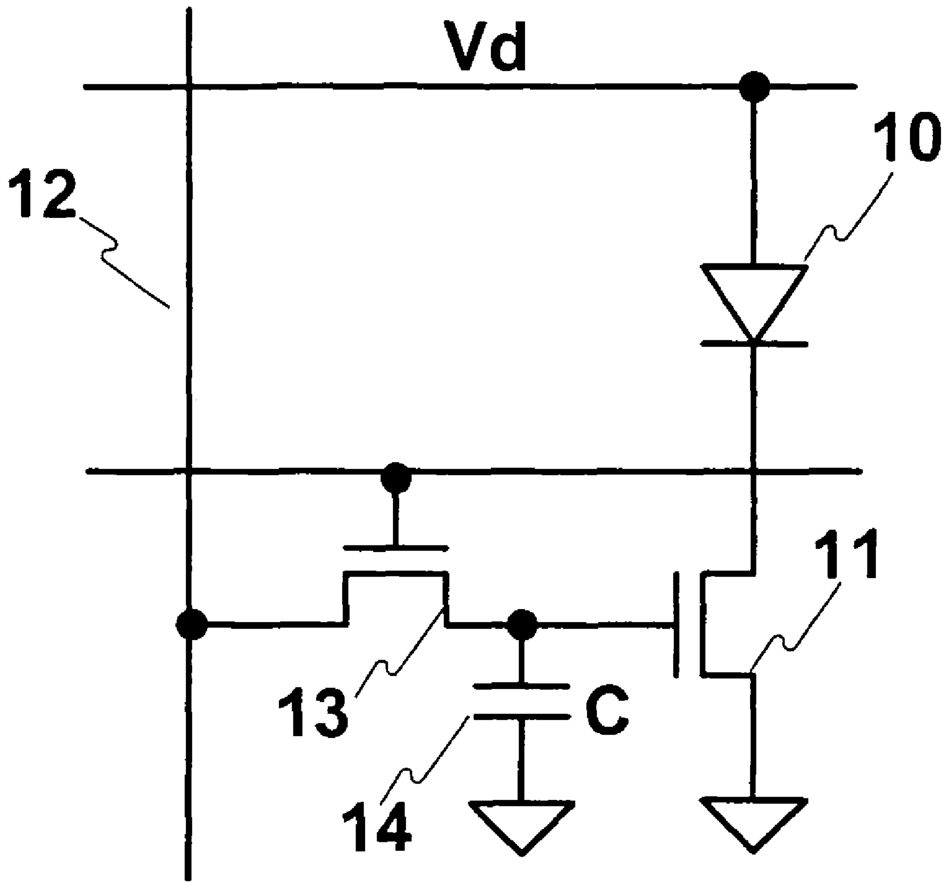

Figure 1

Prior Art

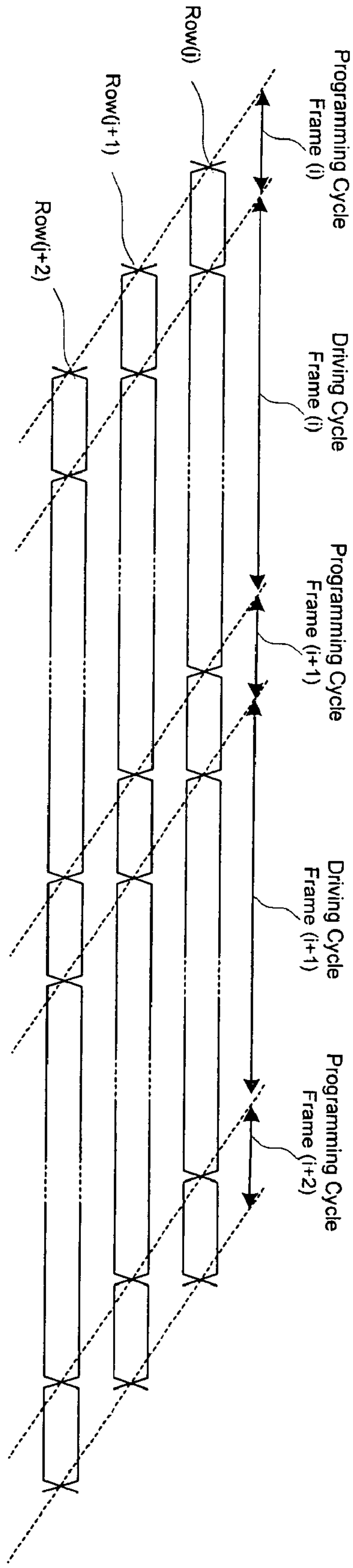
Programming Cycle
Frame (i)
Driving Cycle
Frame (i)
Programming Cycle
Frame (i+1)
Driving Cycle
Frame (i+1)
Programming Cycle
Frame (i+2)
Row(j)
Row(j+1)
Row(j+2)

Figure 2

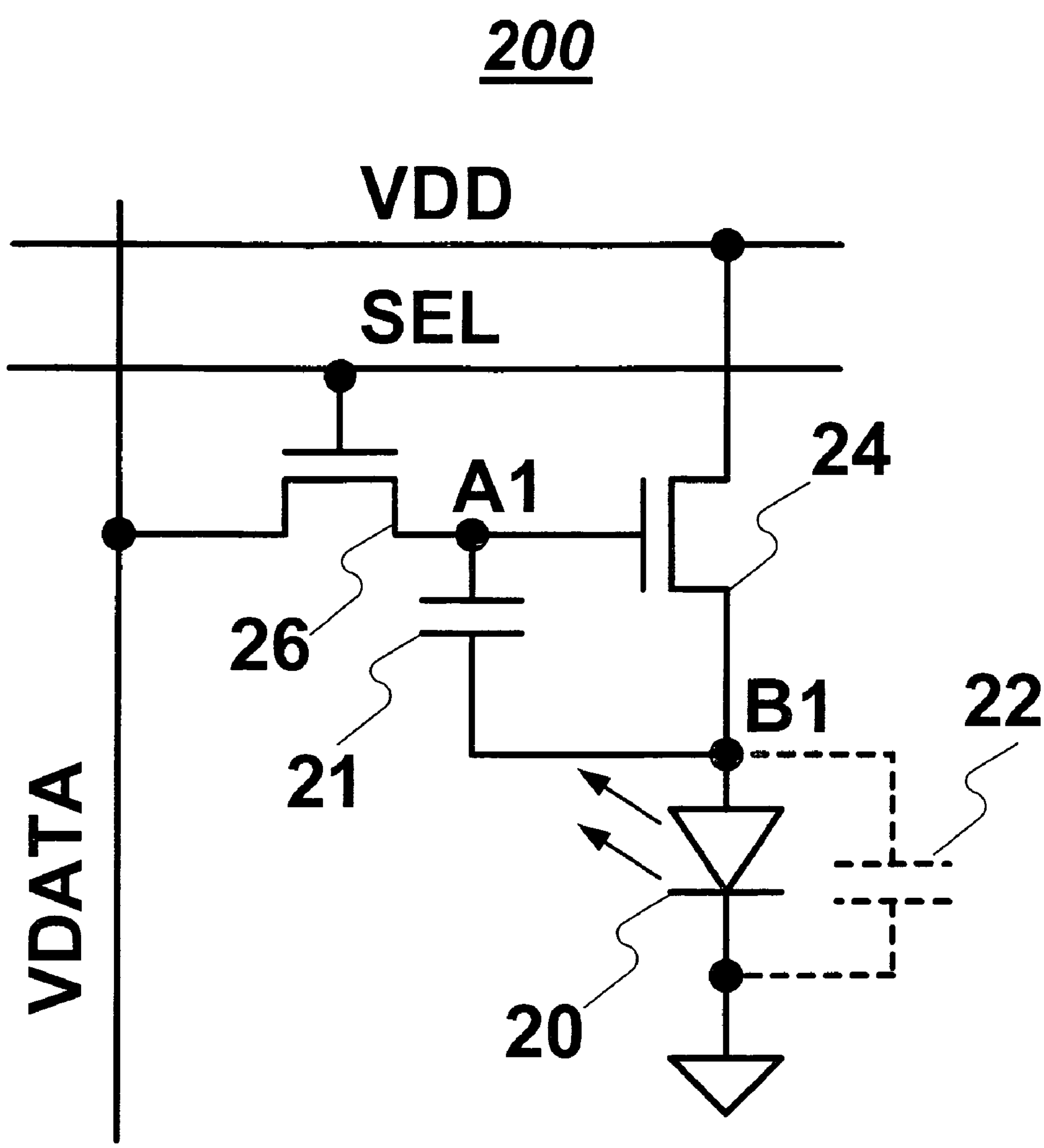

Figure 3

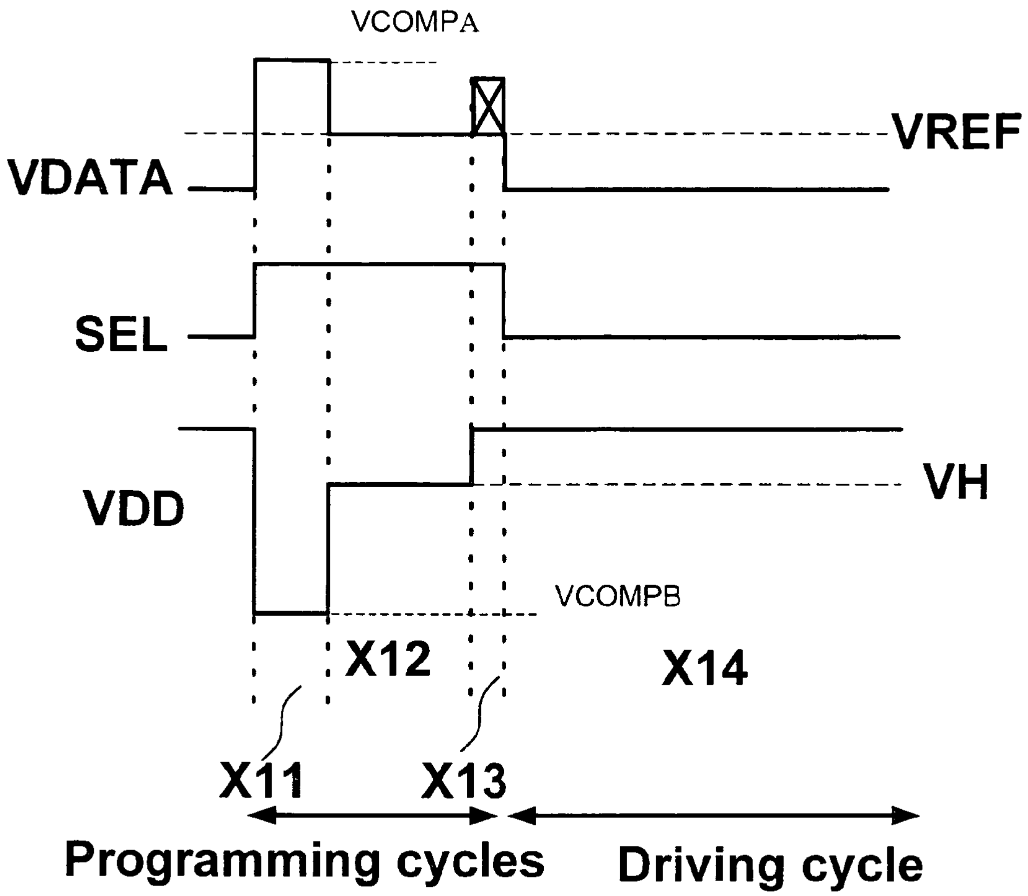
VCOMPA
VREF
VDATA
SEL
VDD
VH
VCOMPB
X12
X14
X11
X13
Programming cycles
Driving cycle

Figure 4

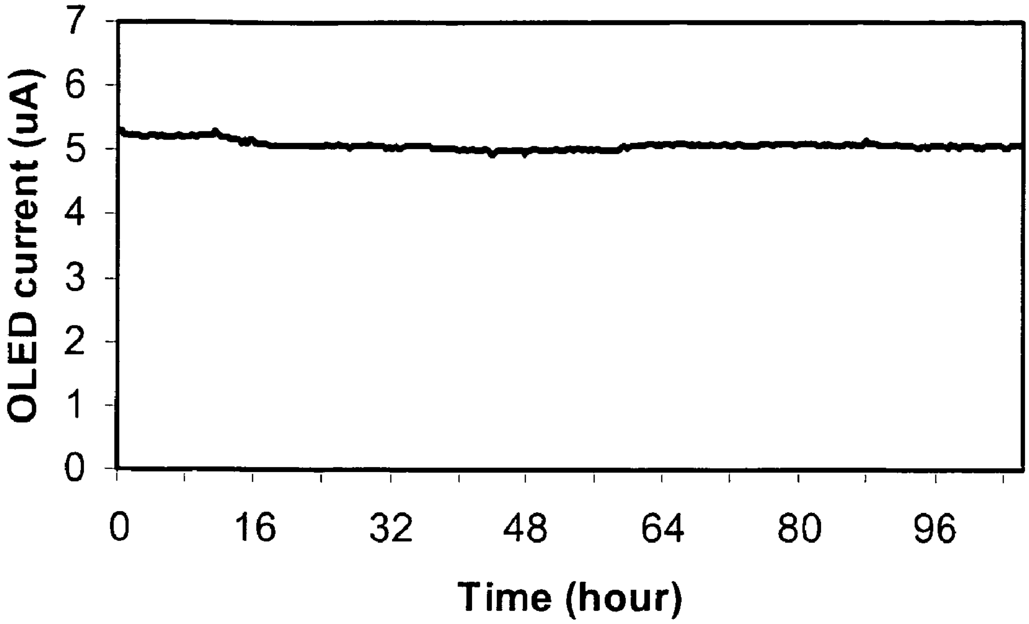

Figure 5

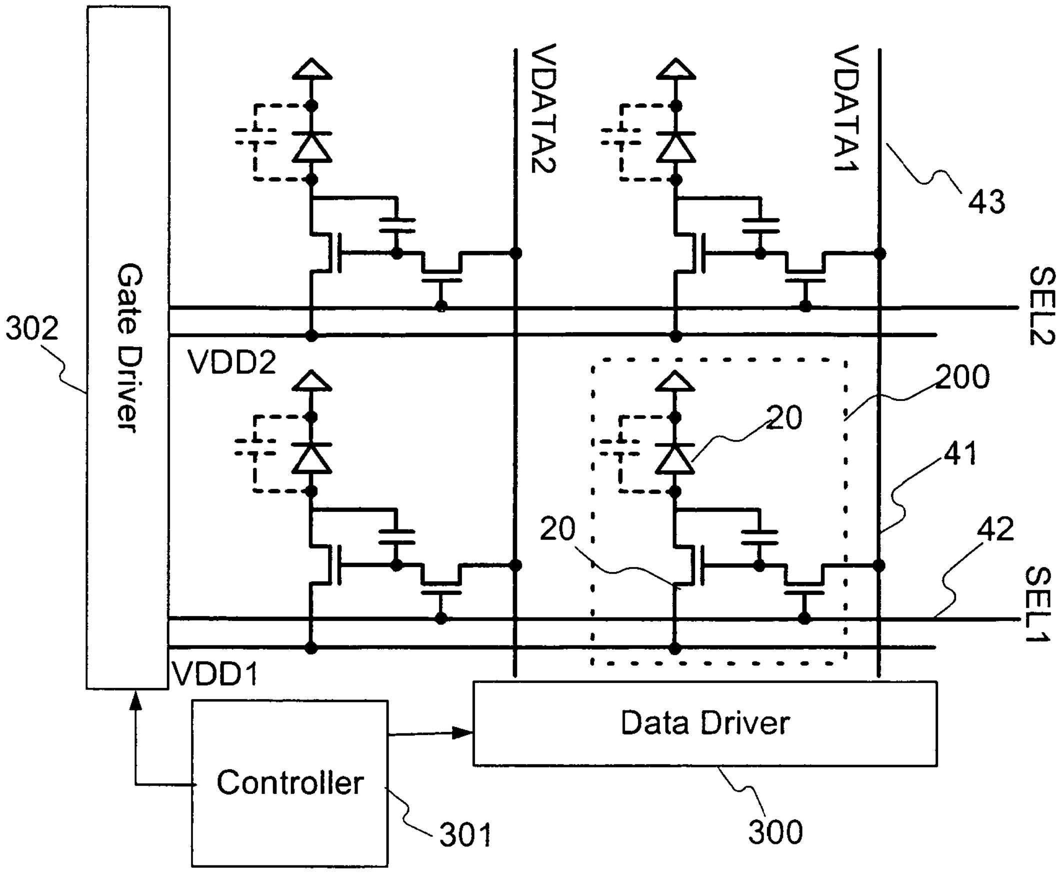
VDATA2
VDATA1
43
SEL2
302
Gate Driver
VDD2
200
20
41
20
42
SEL1
VDD1
Data Driver
Controller
301
300

Figure 6

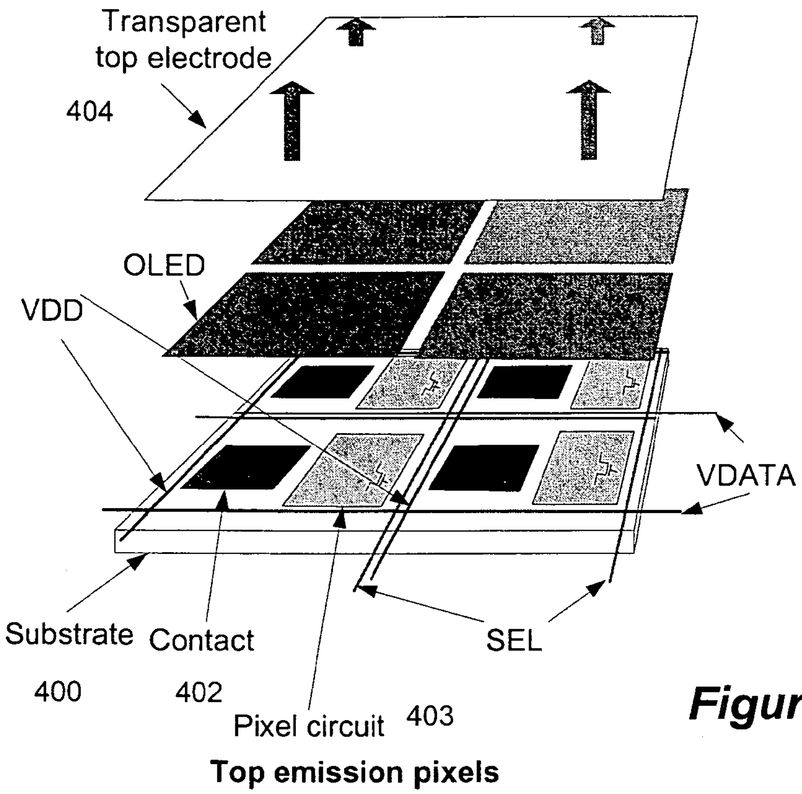

Figure 7(a)

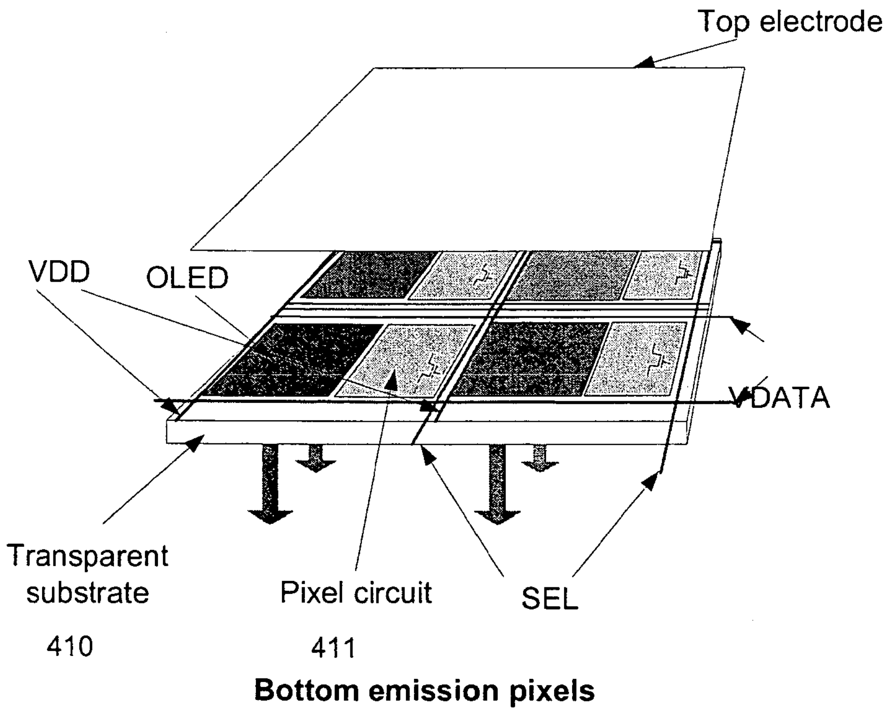

Figure 7(b)

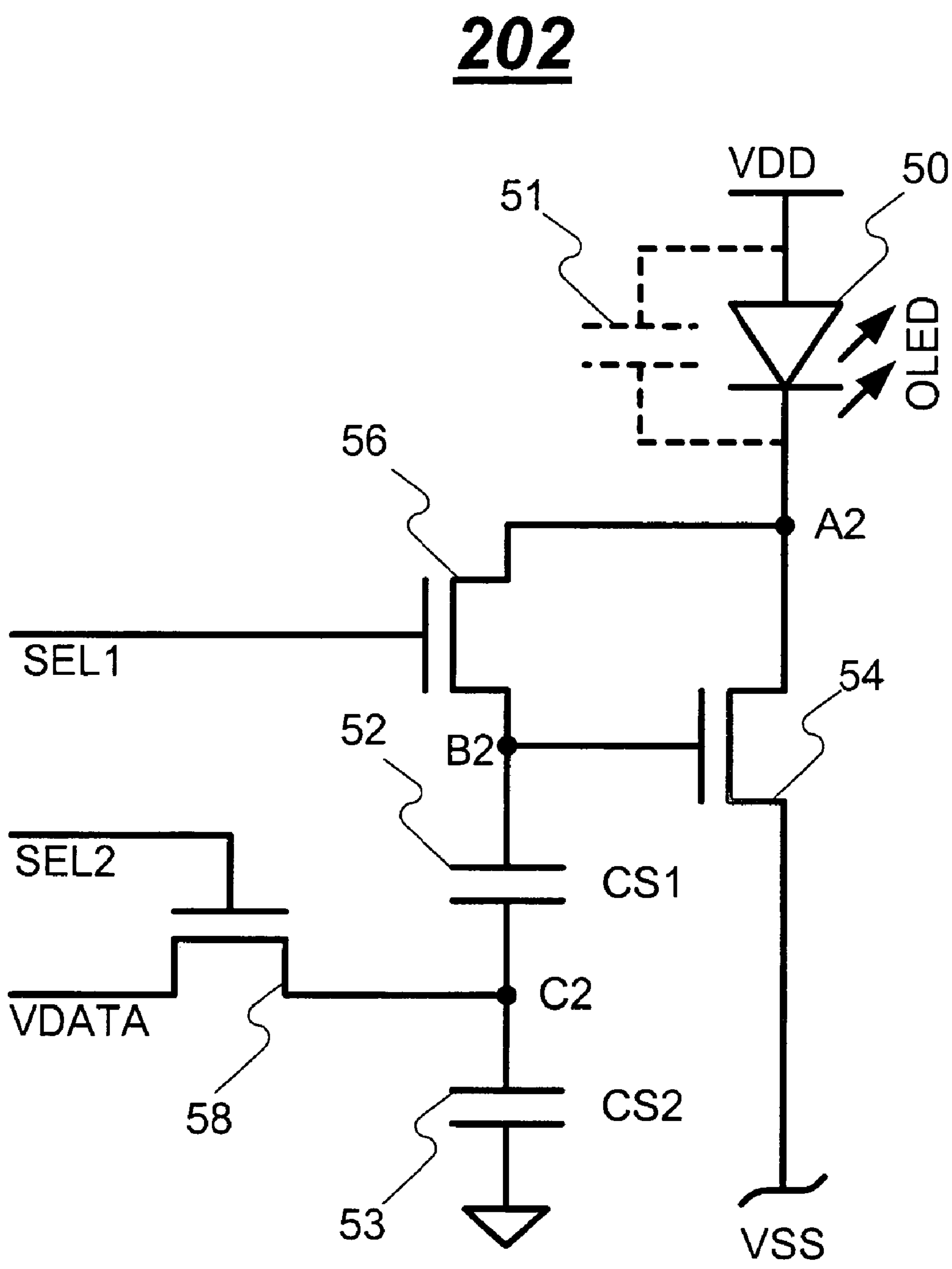
202
VDD
50
51
OLED
56
A2
SEL1
54
52
B2
SEL2
CS1
C2
VDATA
58
CS2
53
VSS

Figure 8

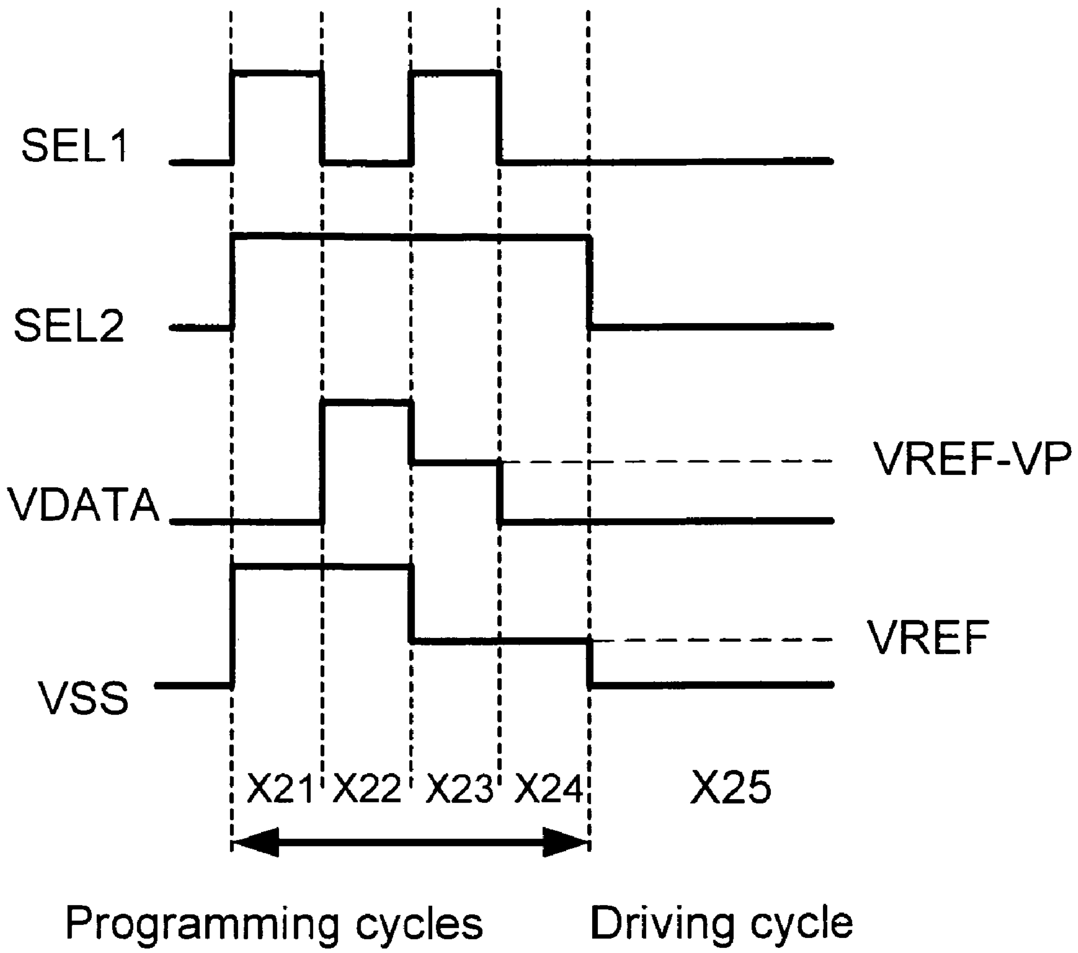
SEL1
SEL2
VDATA
VREF-VP
VSS
VREF
X21
X22
X23
X24
X25
Programming cycles
Driving cycle

Figure 9

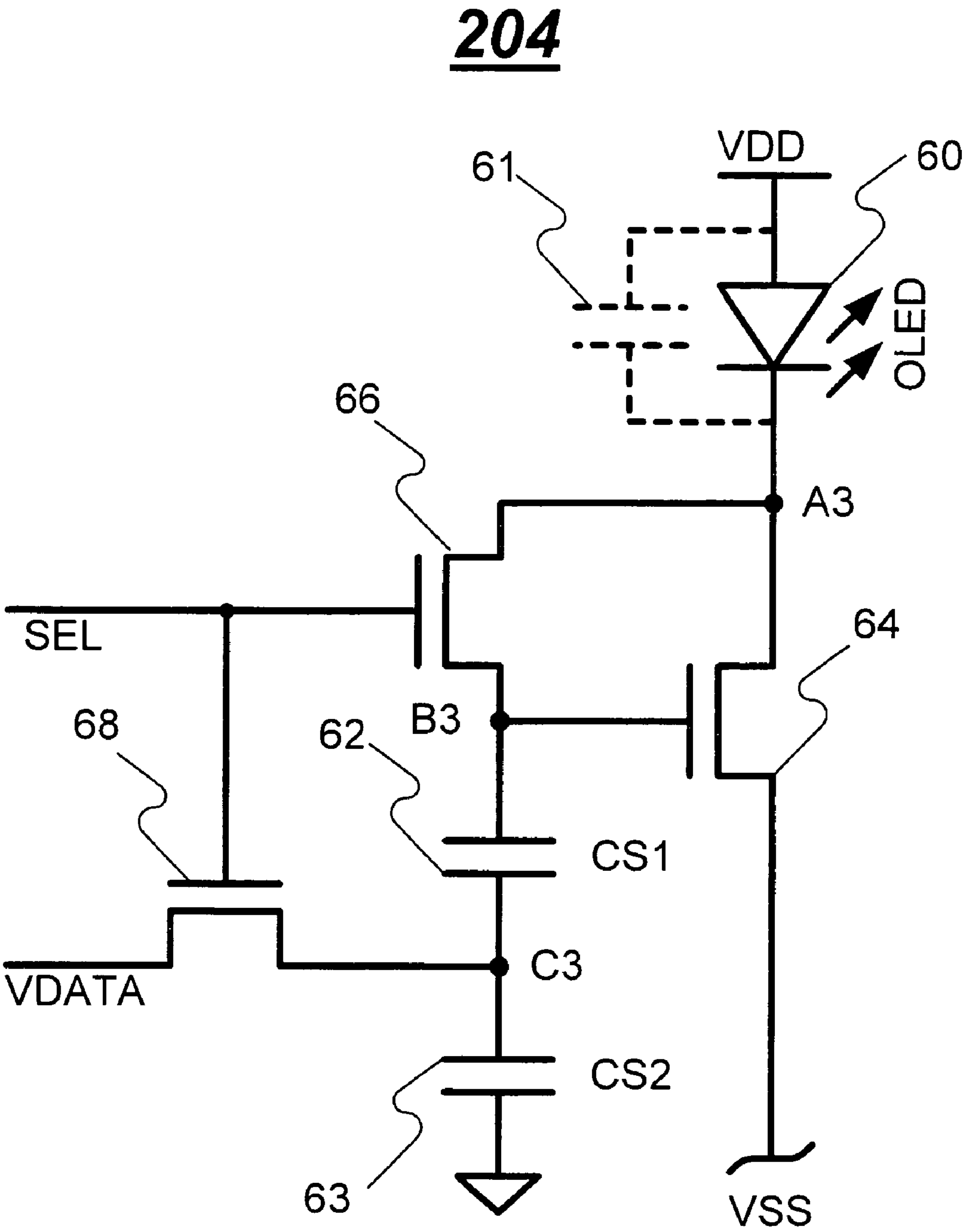

Figure 10

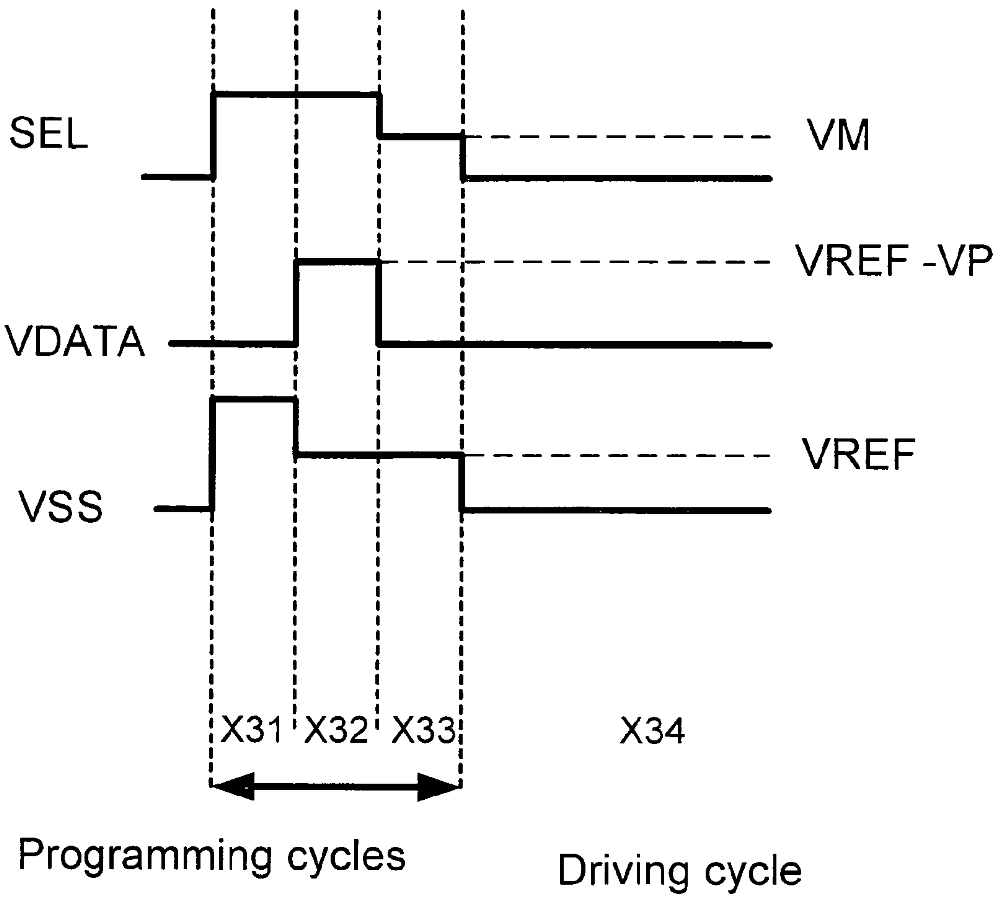
SEL
VM
VREF -VP
VDATA
VREF
VSS
X31
X32
X33
X34
Programming cycles
Driving cycle

Figure 11

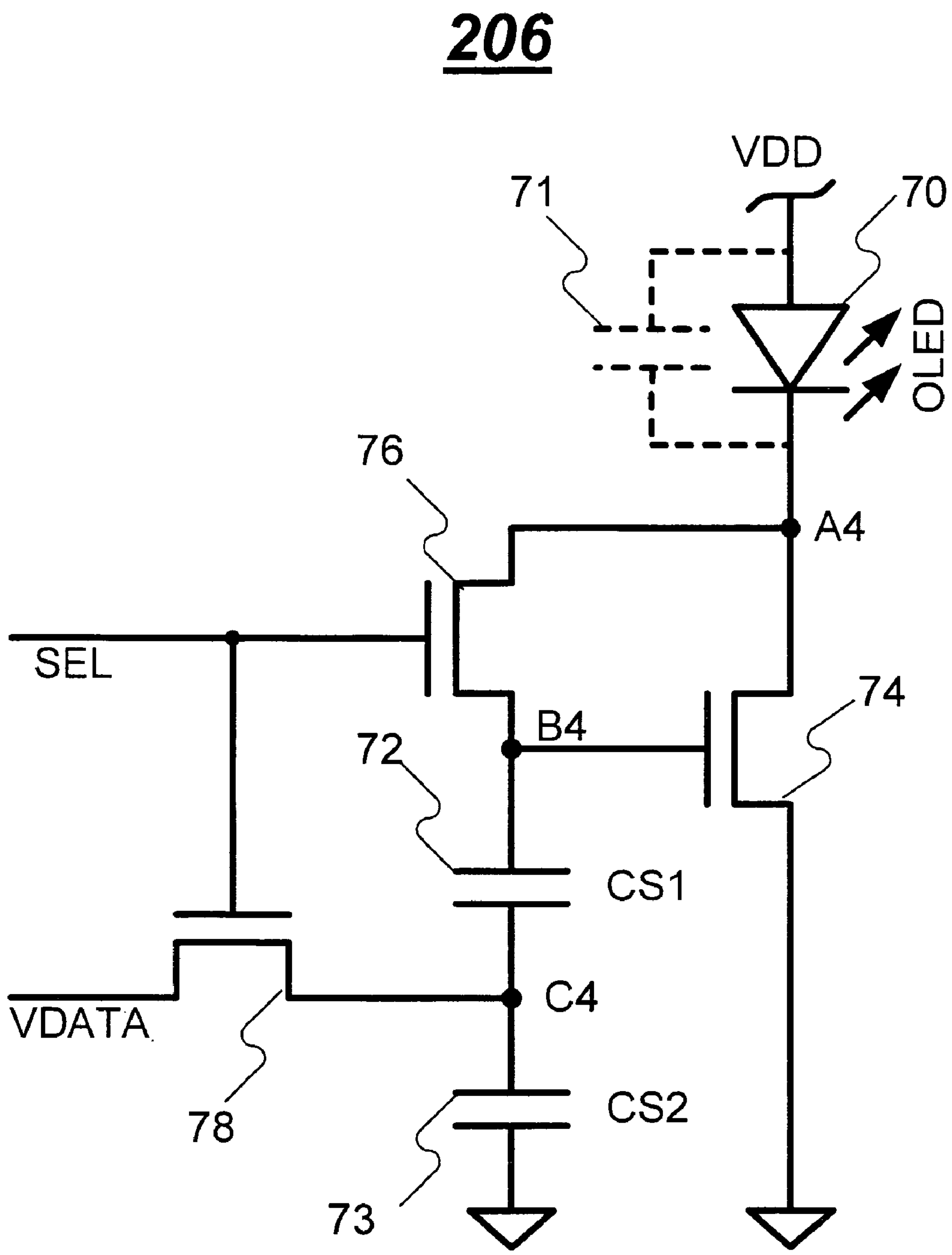

Figure 12

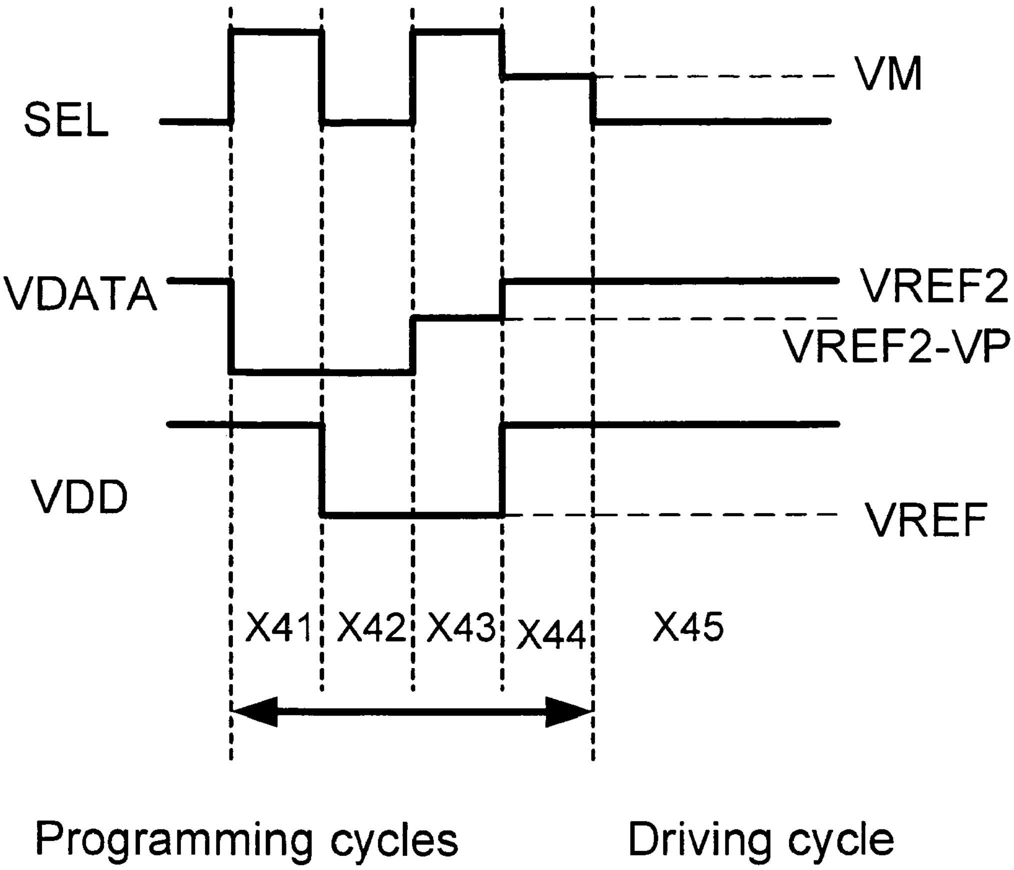
SEL
VM
VDATA
VREF2
VREF2-VP
VDD
VREF
X41
X42
X43
X44
X45
Programming cycles
Driving cycle

Figure 13

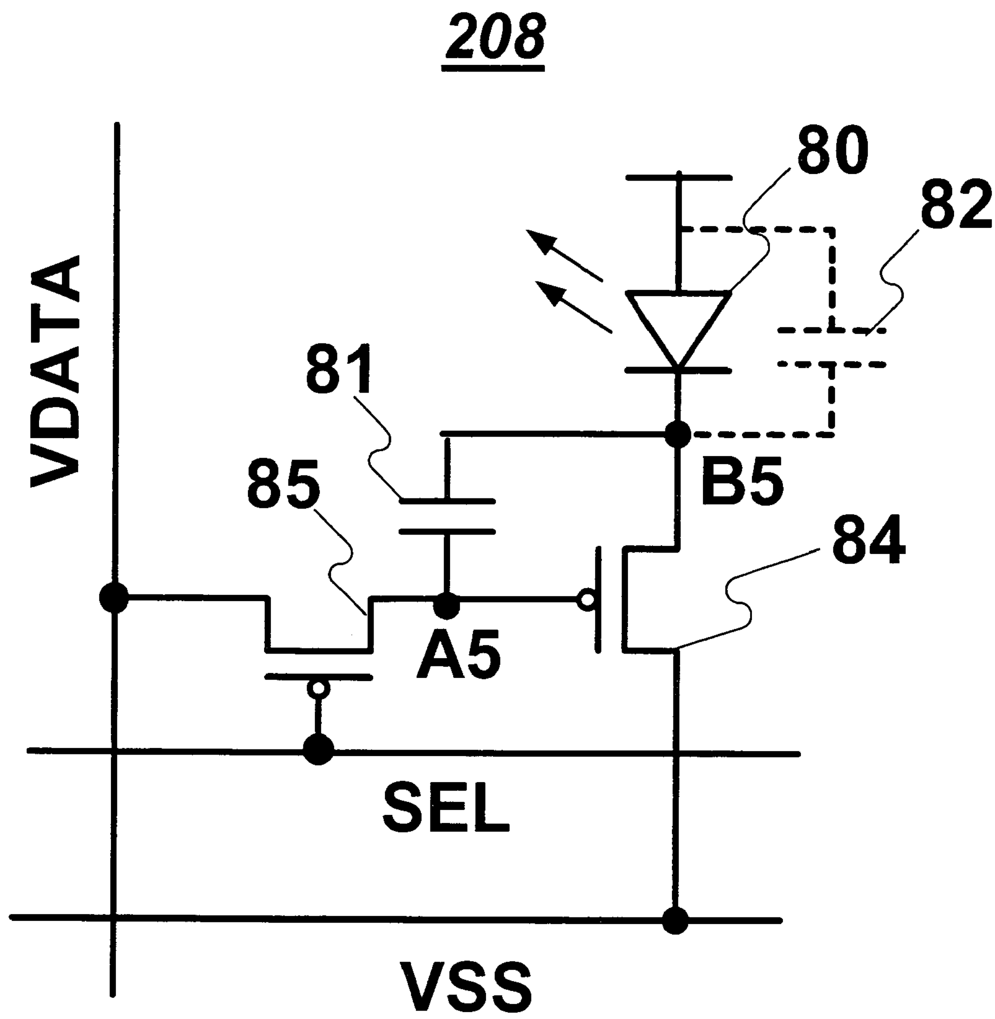

Figure 14

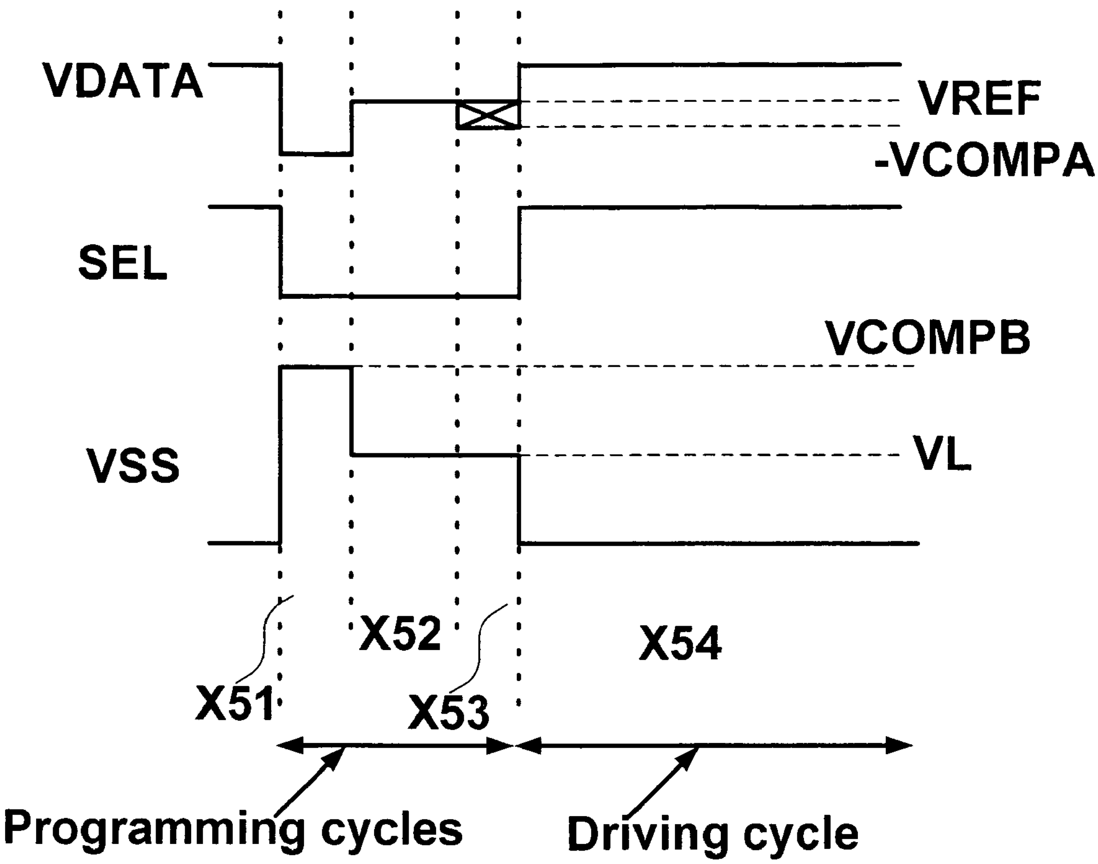
VDATA
VREF
-VCOMPA
SEL
VCOMPB
VSS
VL
X51
X52
X53
X54
Programming cycles
Driving cycle

Figure 15

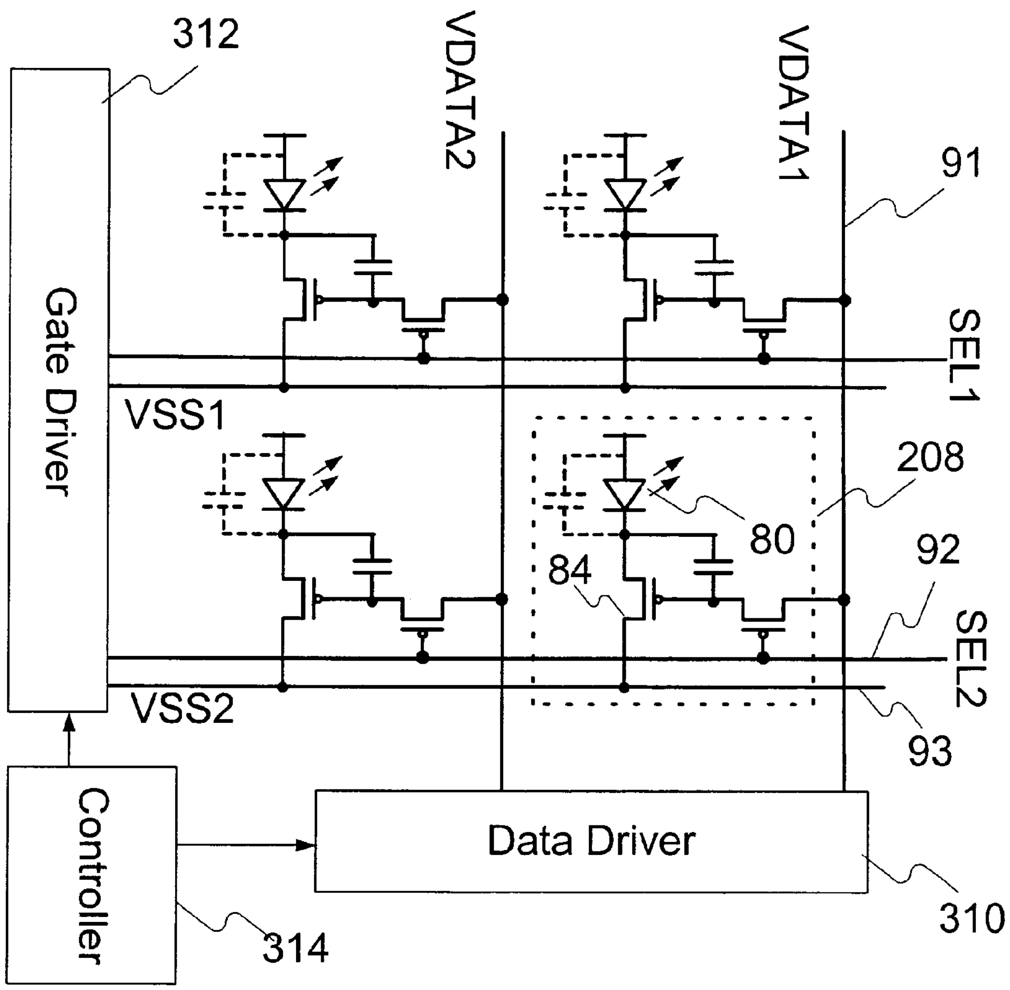
312
VDATA2
VDATA1
91
Gate Driver
SEL1
VSS1
208
80
92
84
SEL2
VSS2
93
Controller
Data Driver
314
310

Figure 16

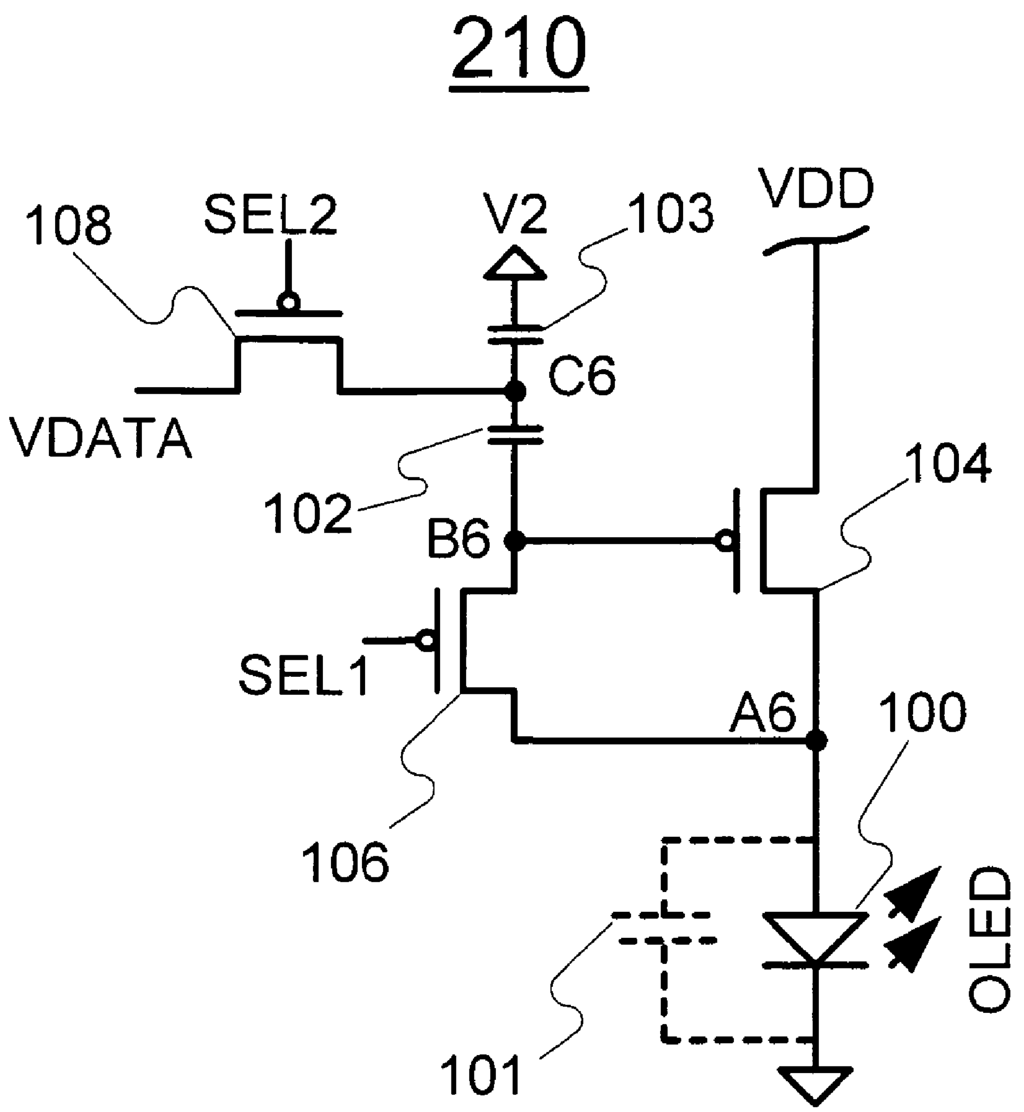
210
108
SEL2
V2
103
VDD
C6
VDATA
102
104
B6
SEL1
A6
100
106
OLED
101

Figure 17

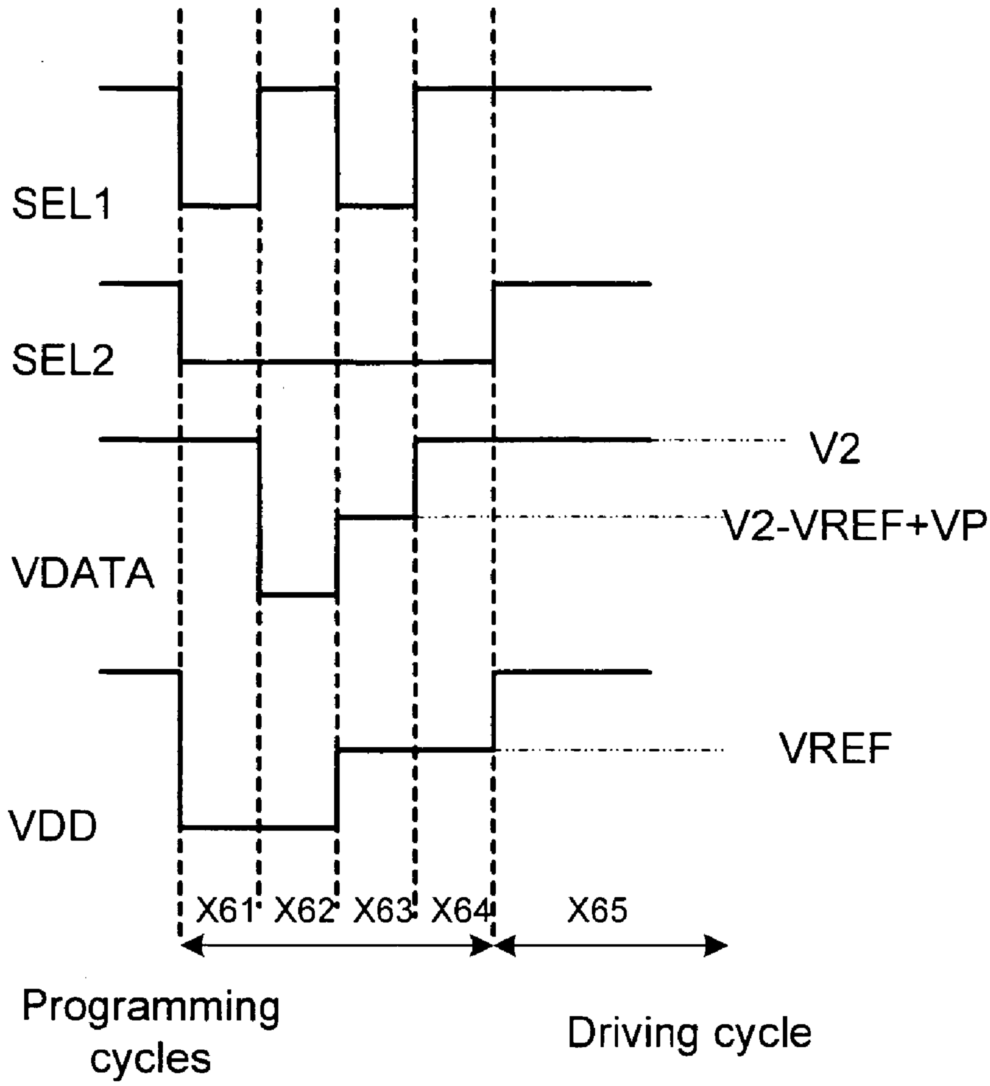
SEL1
SEL2
VDATA
VDD
V2
V2-VREF+VP
VREF
X61
X62
X63
X64
X65
Programming cycles
Driving cycle

Figure 18

212

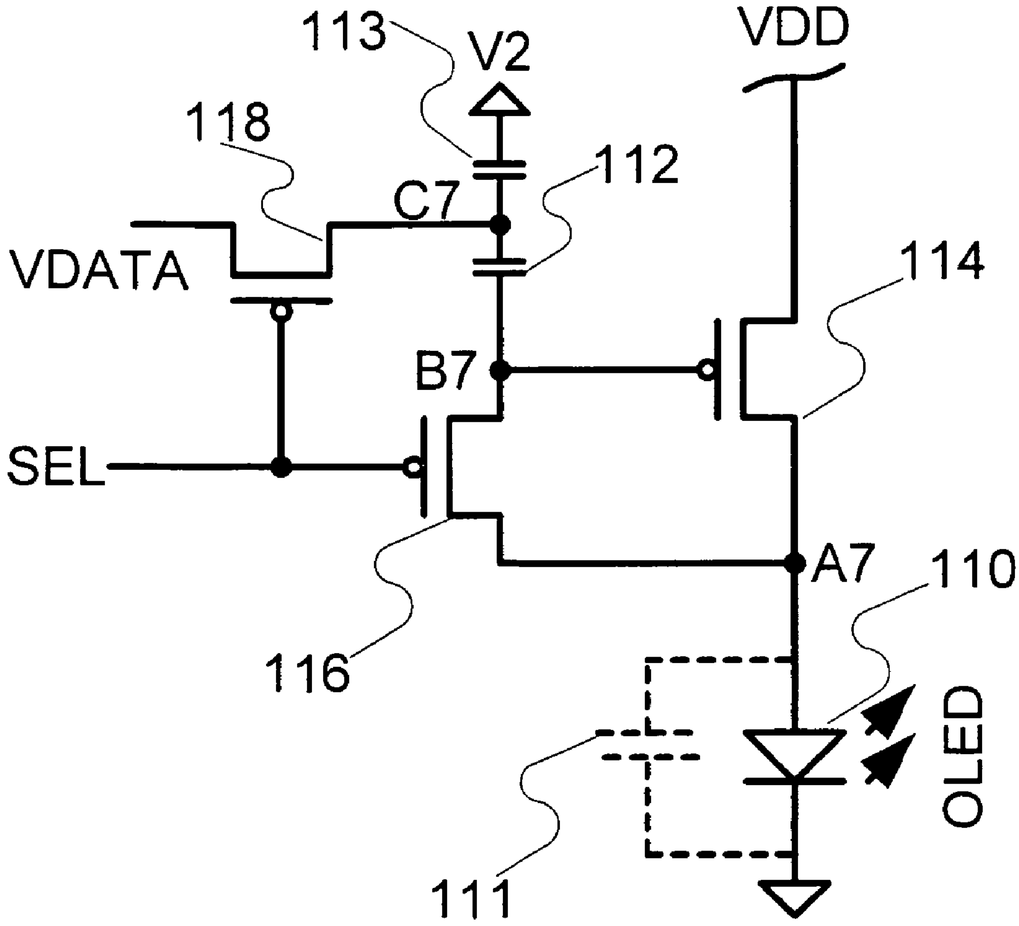

Figure 19

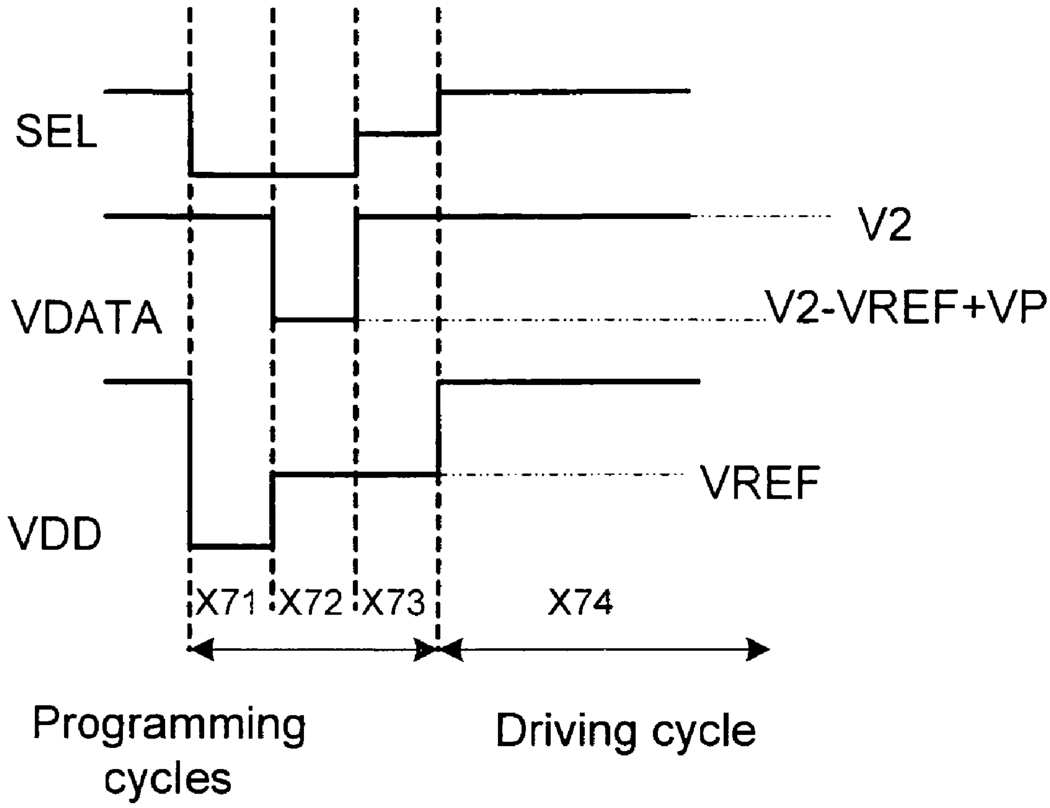
SEL
V2
VDATA
V2-VREF+VP
VDD
VREF
X71
X72
X73
X74
Programming cycles
Driving cycle

Figure 20

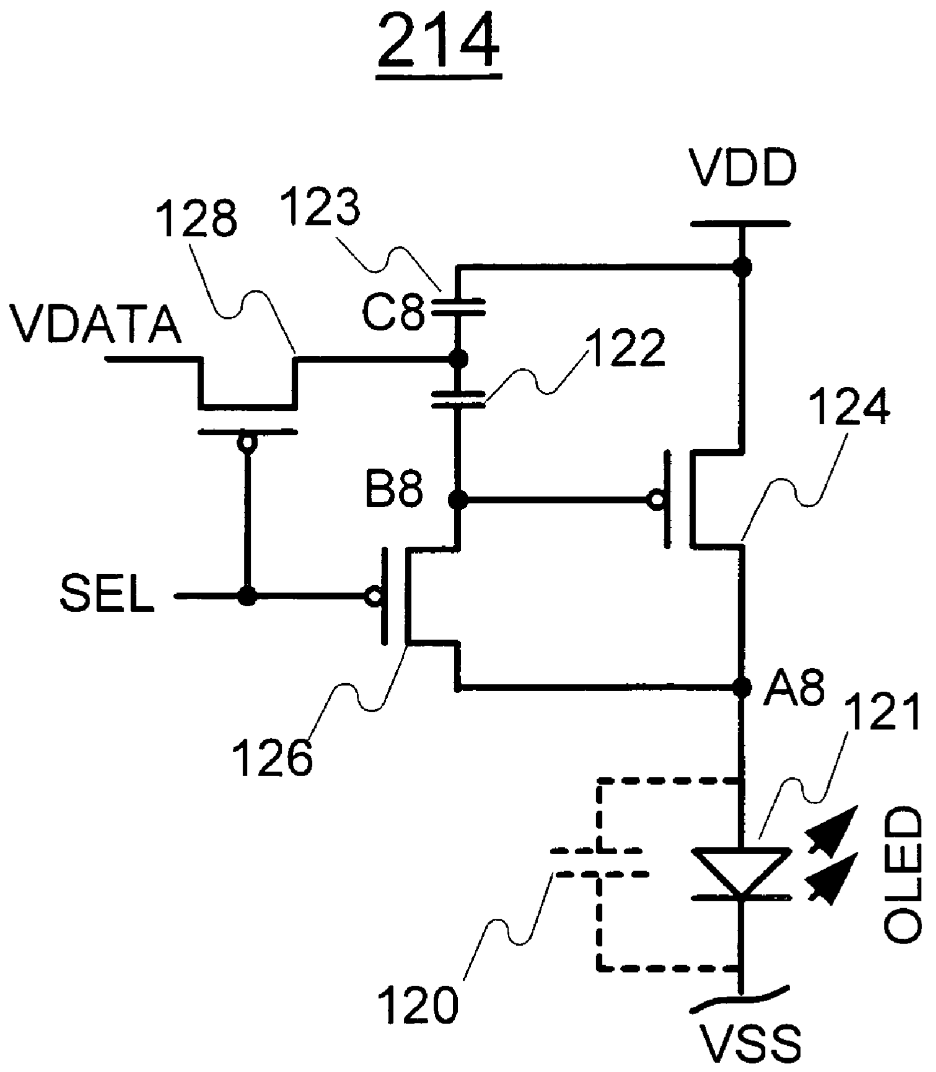

Figure 21

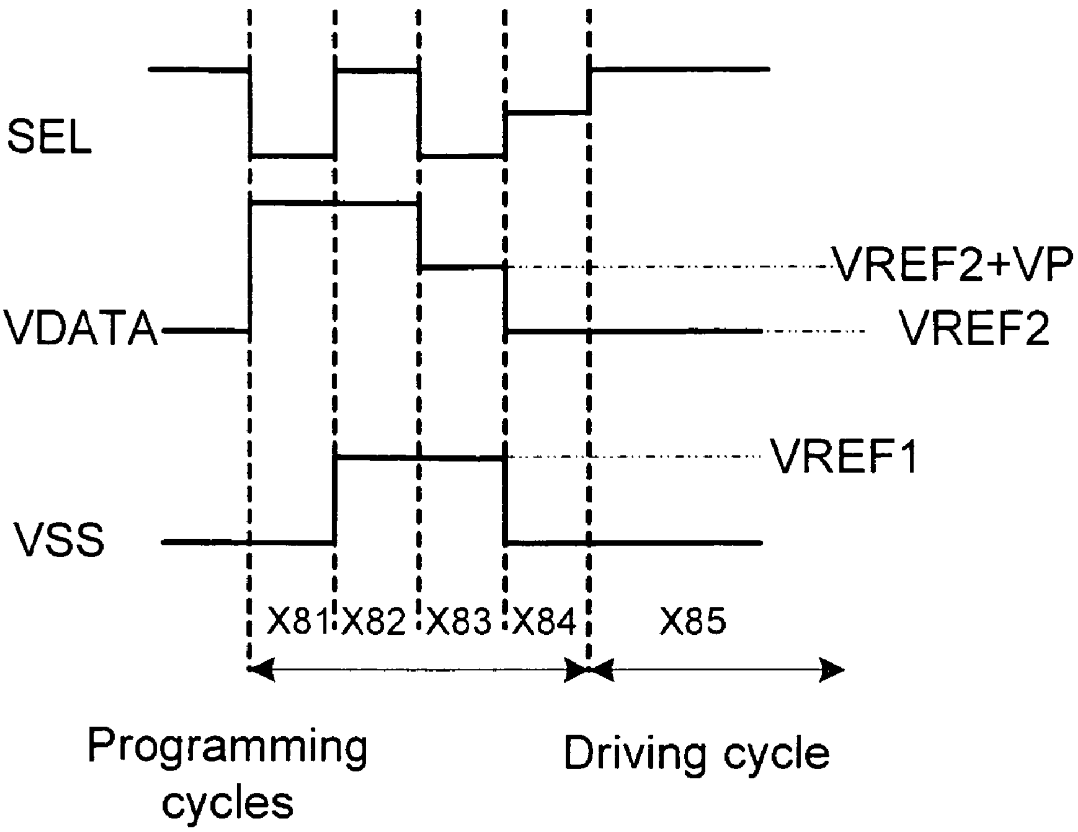
SEL
VDATA
VREF2+VP
VREF2
VREF1
VSS
X81
X82
X83
X84
X85
Programming cycles
Driving cycle

Figure 22

METHOD AND SYSTEM FOR PROGRAMMING AND DRIVING ACTIVE MATRIX LIGHT EMITTING DEVICE PIXEL HAVING A CONTROLLABLE SUPPLY VOLTAGE

CROSS REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. patent application Ser. No. 12/851,652, filed Aug. 6, 2010; which is a continuation of U.S. patent application Ser. No. 11/298,240, filed Dec. 7, 2005, now issued as U.S. Pat. No. 7,800,565, which claims priority to Canadian Patent No. 2,490,858, filed Dec. 7, 2004, each of which is incorporated herein by reference in its entirety.

FIELD OF INVENTION

The present invention relates to a light emitting device displays, and more specifically to a driving technique for the light emitting device displays.

BACKGROUND OF THE INVENTION

Recently active-matrix organic light-emitting diode (AMOLED) displays with amorphous silicon (a-Si), poly-silicon, organic, or other driving backplane have become more attractive due to advantages over active matrix liquid crystal displays. An AMOLED display using a-Si backplanes, for example, has the advantages which include low temperature fabrication that broadens the use of different substrates and makes flexible displays feasible, and its low cost fabrication that yields high resolution displays with a wide viewing angle.

The AMOLED display includes an array of rows and columns of pixels, each having an organic light-emitting diode (OLED) and backplane electronics arranged in the array of rows and columns. Since the OLED is a current driven device, the pixel circuit of the AMOLED should be capable of providing an accurate and constant drive current.

FIG. **1** shows a pixel circuit as disclosed in U.S. Pat. No. 5,748,160. The pixel circuit of FIG. **1** includes an OLED **10**, a driving thin film transistor (TFT) **11**, a switch TFT **13**, and a storage capacitor **14**. The drain terminal of the driving TFT **11** is connected to the OLED **10**. The gate terminal of the driving TFT **11** is connected to a column line **12** through the switch TFT **13**. The storage capacitor **14**, which is connected between the gate terminal of the driving TFT **11** and the ground, is used to maintain the voltage at the gate terminal of the driving TFT **11** when the pixel circuit is disconnected from the column line **12**. The current through the OLED **10** strongly depends on the characteristic parameters of the driving TFT **11**. Since the characteristic parameters of the driving TFT **11**, in particular the threshold voltage under bias stress, vary by time, and such changes may differ from pixel to pixel, the induced image distortion may be unacceptably high.

U.S. Pat. No. 6,229,508 discloses a voltage-programmed pixel circuit which provides, to an OLED, a current independent of the threshold voltage of a driving TFT. In this pixel, the gate-source voltage of the driving TFT is composed of a programming voltage and the threshold voltage of the driving TFT. A drawback of U.S. Pat. No. 6,229,508 is that the pixel circuit requires extra transistors, and is complex, which results in a reduced yield, reduced pixel aperture, and reduced lifetime for the display.

Another method to make a pixel circuit less sensitive to a shift in the threshold voltage of the driving transistor is to use current programmed pixel circuits, such as pixel circuits disclosed in U.S. Pat. No. 6,734,636. In the conventional current programmed pixel circuits, the gate-source voltage of the driving TFT is self-adjusted based on the current that flows through it in the next frame, so that the OLED current is less dependent on the current-voltage characteristics of the driving TFT. A drawback of the current-programmed pixel circuit is that an overhead associated with low programming current levels arises from the column line charging time due to the large line capacitance.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a method and system that obviates or mitigates at least one of the disadvantages of existing systems.

In accordance with an aspect to the present invention there is provided a method of programming and driving a display system, the display system includes: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a capacitor having a first terminal and a second terminal; a switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the switch transistor being connected to a select line, the first terminal of the switch transistor being connected to a signal line for transferring voltage data, the second terminal of the switch transistor being connected to the first terminal of the capacitor; and a driving transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the driving transistor being connected to the second terminal of the switch transistor and the first terminal of the capacitor at a first node (A), the first terminal of the driving transistor being connected to the second terminal of the light emitting device and the second terminal of the capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; a driver for driving the select line, the controllable voltage supply line and the signal line to operate the display array; the method including the steps of: at a programming cycle, at a first operating cycle, charging the second node at a first voltage defined by (VREF−VT) or (−VREF+VT), where VREF represents a reference voltage and VT represents a threshold voltage of the driving transistor; at a second operating cycle, charging the first node at a second voltage defined by (VREF+VP) or (−VREF+VP) so that the difference between the first and second node voltages is stored in the storage capacitor, where VP represents a programming voltage; at a driving cycle, applying the voltage stored in the storage capacitor to the gate terminal of the driving transistor.

In accordance with a further aspect to the present invention there is provided a method of programming and driving a display system, the display system includes: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a first capacitor and a second capacitor, each having a first terminal and a second terminal; a first switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the first switch transistor being connected to a first select line, the first terminal of the first switch transistor being connected to the second terminal of the light emitting device, the second terminal of the first switch being connected to the first terminal of the first capacitor; a second switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the second switch transistor being connected to a second select line, the first terminal of the second switch transistor being connected to a signal line for transferring voltage data; a driving transistor having a gate terminal, a first terminal and a second terminal, the first terminal of the driving transistor being connected to the second terminal of the light emitting device at a first node (A), the gate terminal of the driving transistor being connected to the second terminal of the first switch transistor and the first terminal of the first capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; the second terminal of the second switch transistor being connected to the second terminal of the first capacitor and the first terminal of the second capacitor at a third node (C); a driver for driving the first and second select line, the controllable voltage supply line and the signal line to operate the display array, the method including the steps of: at a programming cycle, at a first operating cycle, controlling the voltage of each of the first node and the second node so as to store (VT+VP) or −(VT+VP) in the first storage capacitor, where VT represents a threshold voltage of the driving transistor, VP represents a programming voltage; at a second operating cycle, discharging the third node; at a driving cycle, applying the voltage stored in the storage capacitor to the gate terminal of the driving transistor.

In accordance with a further aspect to the present invention there is provided a display system including: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a capacitor having a first terminal and a second terminal; a switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the switch transistor being connected to a select line, the first terminal of the switch transistor being connected to a signal line for transferring voltage data, the second terminal of the switch transistor being connected to the first terminal of the capacitor; and a driving transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the driving transistor being connected to the second terminal of the switch transistor and the first terminal of the capacitor at a first node (A), the first terminal of the driving transistor being connected to the second terminal of the light emitting device and the second terminal of the capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; a driver for driving the select line, the controllable voltage supply line and the signal line to operate the display array; and a controller for implementing a programming cycle and a driving cycle on each row of the display array using the driver; wherein the programming cycle includes a first operating cycle and a second operating cycle, wherein at the first operating cycle, the second node is charged at a first voltage defined by (VREF−VT) or (−VREF+VT), where VREF represents a reference voltage and VT represents a threshold voltage of the driving transistor, at the second operating cycle, the first node is charged at a second voltage defined by (VREF+VP) or (−VREF+VP) so that the difference between the first and second node voltages is stored in the storage capacitor, where VP represents a programming voltage; wherein at the driving cycle, the voltage stored in the storage capacitor is applied to the gate terminal of the driving transistor.

In accordance with a further aspect to the present invention there is provided a display system including: a display array having a plurality of pixel circuits arranged in row and column, each pixel circuit having: a light emitting device having a first terminal and a second terminal, the first terminal of the lighting device being connected to a voltage supply electrode; a first capacitor and a second capacitor, each having a first terminal and a second terminal; a first switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the first switch transistor being connected to a first select line, the first terminal of the first switch transistor being connected to the second terminal of the light emitting device, the second terminal of the first switch being connected to the first terminal of the first capacitor; a second switch transistor having a gate terminal, a first terminal and a second terminal, the gate terminal of the second switch transistor being connected to a second select line, the first terminal of the second switch transistor being connected to a signal line for transferring voltage data; a driving transistor having a gate terminal, a first terminal and a second terminal, the first terminal of the driving transistor being connected to the second terminal of the light emitting device at a first node (A), the gate terminal of the driving transistor being connected to the second terminal of the first switch transistor and the first terminal of the first capacitor at a second node (B), the second terminal of the driving transistor being connected to a controllable voltage supply line; the second terminal of the second switch transistor being connected to the second terminal of the first capacitor and the first terminal of the second capacitor at a third node (C); a driver for driving the first and second select line, the controllable voltage supply line and the signal line to operate the display array; and a controller for implementing a programming cycle and a driving cycle on each row of the display array using the driver; wherein the programming cycle includes a first operating cycle and a second operating cycle, wherein at the first operating cycle, the voltage of each of the first node and the second node is controlled so as to store (VT+VP) or −(VT+VP) in the first storage capacitor, where VT represents a threshold voltage of the driving transistor, VP represents a programming voltage, at the second operating cycle, the third node is discharged, wherein at the driving cycle, the voltage stored in the storage capacitor is applied to the gate terminal of the driving transistor.

This summary of the invention does not necessarily describe all features of the invention.

Other aspects and features of the present invention will be readily apparent to those skilled in the art from a review of the following detailed description of preferred embodiments in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings wherein:

FIG. **1** is a diagram showing a conventional 2-TFT voltage programmed pixel circuit;

FIG. **2** is a timing diagram showing an example of programming and driving cycles in accordance with an embodiment of the present invention, which is applied to a display array;

FIG. **3** is a diagram showing a pixel circuit to which programming and driving technique in accordance with an embodiment of the present invention is applied;

FIG. **4** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **3**;

FIG. **5** is a diagram showing a lifetime test result for the pixel circuit of FIG. **3**;

FIG. **6** is a diagram showing a display system having the pixel circuit of FIG. **3**;

FIG. **7**(*a*) is a diagram showing an example of the array structure having top emission pixels which are applicable to the array of FIG. **6**;

FIG. **7**(*b*) is a diagram showing an example of the array structure having bottom emission pixels which are applicable to the array of FIG. **6**;

FIG. **8** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

FIG. **9** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **8**;

FIG. **10** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

FIG. **11** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **10**;

FIG. **12** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

FIG. **13** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **12**;

FIG. **14** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

FIG. **15** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **14**;

FIG. **16** is a diagram showing a display system having the pixel circuit of FIG. **14**;

FIG. **17** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

FIG. **18** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **17**;

FIG. **19** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied;

FIG. **20** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **19**;

FIG. **21** is a diagram showing a pixel circuit to which programming and driving technique in accordance with a further embodiment of the present invention is applied; and

FIG. **22** is a timing diagram showing an example of waveforms for programming and driving the pixel circuit of FIG. **21**;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS OF THE INVENTION

Embodiments of the present invention are described using a pixel having an organic light emitting diode (OLED) and a driving thin film transistor (TFT). However, the pixel may include any light emitting device other than OLED, and the pixel may include any driving transistor other than TFT. It is noted that in the description, "pixel circuit" and "pixel" may be used interchangeably.

FIG. **2** is a diagram showing programming and driving cycles in accordance with an embodiment of the present invention. In FIG. **2**, each of ROW(j), ROW(j+1), and ROW (j+2) represents a row of the display array where a plurality of pixel circuits are arranged in row and column.

The programming and driving cycle for a frame occurs after the programming and driving cycle for a next frame. The programming and driving cycles for the frame at a ROW overlaps with the programming and driving cycles for the same frame at a next ROW. As described below, during the programming cycle, the time depending parameter(s) of the pixel circuit is extracted to generate a stable pixel current.

FIG. **3** illustrates a pixel circuit **200** to which programming and driving technique in accordance with an embodiment of the present invention is applied. The pixel circuit **200** includes an OLED **20**, a storage capacitor **21**, a driving transistor **24**, and a switch transistor **26**. The pixel circuit **200** is a voltage programmed pixel circuit. Each of the transistors **24** and **26** has a gate terminal, a first terminal and a second terminal. In the description, the first terminal (second terminal) may be, but not limited to, a drain terminal or a source terminal (a source terminal or a drain terminal).

The transistors **24** and **26** are n-type TFTs. However, the transistors **24** and **26** may be p-type transistors. As described below, the driving technique applied to the pixel circuit **200** is also applicable to a complementary pixel circuit having p-type transistors as shown in FIG. **14**. The transistors **24** and **26** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

The first terminal of the driving transistor **24** is connected to a controllable voltage supply line VDD. The second terminal of the driving transistor **24** is connected to the anode electrode of the OLED **20**. The gate terminal of the driving transistor **24** is connected to a signal line VDATA through the switch transistor **26**. The storage capacitor **21** is connected between the source and gate terminals of the driving transistor **24**.

The gate terminal of the switch transistor **26** is connected to a select line SEL. The first terminal of the switch transistor **26** is connected to the signal line VDATA. The second terminal of the switch transistor **26** is connected to the gate terminal of the driving transistor **24**. The cathode electrode of the OLED **20** is connected to a ground voltage supply electrode.

The transistors **24** and **26** and the storage capacitor **21** are connected at node A**1**. The transistor **24**, the OLED **20** and the storage capacitor **21** are connected at node B**1**.

FIG. **4** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **200** of FIG. **3**. Referring to FIGS. **3** and **4**, the operation of the pixel circuit **200** includes a programming cycle having three operating cycles X**11**, X**12** and X**13**, and a driving cycle having one operating cycle X**14**.

During the programming cycle, node B**1** is charged to the negative threshold voltage of the driving transistor **24**, and node A**1** is charged to a programming voltage VP.

As a result, the gate-source voltage of the driving transistor **24** goes to:

$$VGS=VP-(-VT)=VP+VT \tag{1}$$

where VGS represents the gate-source voltage of the driving transistor **24**, and VT represents the threshold voltage of the driving transistor **24**.

Since the driving transistor **24** is in saturation regime of operation, its current is defined mainly by its gate-source voltage. As a result the current of the driving transistor **24** remains constant even if the OLED voltage changes, since its gate-source voltage is stored in the storage capacitor **21**.

In the first operating cycle X11: VDD goes to a compensating voltage VCOMPB, and VDATA goes to a high positive compensating voltage VCOMPA, and SEL is high. As a result, node A1 is charged to VCOMPA and node B1 is charged to VCOMPB.

In the second operating cycle X12: While VDATA goes to a reference voltage VREF, node B1 is discharged through the driving transistor 24 until the driving transistor 24 turns off. As a result, the voltage of node B1 reaches (VREF−VT). VDD has a positive voltage VH to increase the speed of this cycle X12. For optimal setting time, VH can be set to be equal to the operating voltage which is the voltage on VDD during the driving cycle.

In the third operating cycle X13: VDD goes to its operating voltage. While SEL is high, node A1 is charged to (VP+VREF). Because the capacitance 22 of the OLED 20 is large, the voltage at node B1 stays at the voltage generated in the previous cycle X12. Thus, the voltage of node B1 is (VREF−VT). Therefore, the gate-source voltage of the driving transistor 24 is (VP+VT), and this gate-source voltage is stored in the storage capacitor 21.

In the fourth operating cycle X14: SEL and VDATA go to zero. VDD is the same as that of the third operating cycle X13. However, VDD may be higher than that of the third operating cycle X13. The voltage stored in the storage capacitor 21 is applied to the gate terminal of the driving transistor 24. Since the gate-source voltage of the driving transistor 24 include its threshold voltage and also is independent of the OLED voltage, the degradation of the OLED 20 and instability of the driving transistor 24 does not affect the amount of current flowing through the driving transistor 24 and the OLED 20.

It is noted that the pixel circuit 200 can be operated with different values of VCOMPB, VCOMPA, VP, VREF and VH. VCOMPB, VCOMPA, VP, VREF and VH define the lifetime of the pixel circuit 200. Thus, these voltages can be defined in accordance with the pixel specifications.

FIG. 5 illustrates a lifetime test result for the pixel circuit and waveform shown in FIGS. 3 and 4. In the test, a fabricated pixel circuit was put under the operation for a long time while the current of the driving transistor (24 of FIG. 3) was monitored to investigate the stability of the driving scheme. The result shows that OLED current is stable after 120-hour operation. The VT shift of the driving transistor is 0.7 V.

FIG. 6 illustrates a display system having the pixel circuit 200 of FIG. 3. VDD1 and VDD2 of FIG. 6 correspond to VDD of FIG. 3. SEL1 and SEL2 of FIG. 6 correspond to SEL of FIG. 3. VDATA1 and VDATA2 of FIG. 6 correspond to VDATA of FIG. 3. The array of FIG. 6 is an active matrix light emitting diode (AMOLED) display having a plurality of the pixel circuits 200 of FIG. 3. The pixel circuits are arranged in rows and columns, and interconnections 41, 42 and 43 (VDATA1, SEL1, VDD1). VDATA1 (or VDATA 2) is shared between the common column pixels while SEL1 (or SEL2) and VDD1 (or VDD2) are shared between common row pixels in the array structure.

A driver 300 is provided for driving VDATA1 and VDATA2. A driver 302 is provided for driving VDD1, VDD2, SEL1 and SEL 2, however, the driver for VDD and SEL lines can also be implemented separately. A controller 304 controls the drivers 300 and 302 to programming and driving the pixel circuits as described above. The timing diagram for programming and driving the display array of FIG. 6 is as shown in FIG. 2. Each programming and driving cycle may be the same as that of FIG. 4.

FIG. 7(*a*) illustrates an example of array structure having top emission pixels are arranged. FIG. 7(*b*) illustrates an example of array structure having bottom emission pixels are arranged. The array of FIG. 6 may have array structure shown in FIG. 7(*a*) or 7(*b*). In FIG. 7(*a*), 400 represents a substrate, 402 represents a pixel contact, 403 represents a (top emission) pixel circuit, and 404 represents a transparent top electrode on the OLEDs. In FIG. 7(*b*), 410 represents a transparent substrate, 411 represents a (bottom emission) pixel circuit, and 412 represents a top electrode. All of the pixel circuits including the TFTs, the storage capacitor, the SEL, VDATA, and VDD lines are fabricated together. After that, the OLEDs are fabricated for all pixel circuits. The OLED is connected to the corresponding driving transistor using a via (e.g. B1 of FIG. 3) as shown in FIGS. 7(*a*) and 7(*b*). The panel is finished by deposition of the top electrode on the OLEDs which can be a continuous layer, reducing the complexity of the design and can be used to turn the entire display ON/OFF or control the brightness.

FIG. 8 illustrates a pixel circuit 202 to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit 202 includes an OLED 50, two storage capacitors 52 and 53, a driving transistor 54, and switch transistors 56 and 58. The pixel circuit 202 is a top emission, voltage programmed pixel circuit. This embodiment principally works in the same manner as that of FIG. 3. However, in the pixel circuit 202, the OLED 50 is connected to the drain terminal of the driving transistor 54. As a result, the circuit can be connected to the cathode of the OLED 50. Thus, the OLED deposition can be started with the cathode.

The transistors 54, 56 and 58 are n-type TFTs. However, the transistors 54, 56 and 58 may be p-type transistors The driving technique applied to the pixel circuit 202 is also applicable to a complementary pixel circuit having p-type transistors as shown in FIG. 17. The transistors 54, 56 and 58 may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

The first terminal of the driving transistor 54 is connected to the cathode electrode of the OLED 50. The second terminal of the driving transistor 54 is connected to a controllable voltage supply line VSS. The gate terminal of the driving transistor 54 is connected to its first line (terminal) through the switch transistor 56. The storage capacitors 52 and 53 are in series, and are connected between the gate terminal of the driving transistor 54 and a common ground. The voltage on the voltage supply line VSS is controllable. The common ground may be connected to VSS.

The gate terminal of the switch transistor 56 is connected to a first select line SEL1. The first terminal of the switch transistor 56 is connected to the drain terminal of the driving transistor 54. The second terminal of the switch transistor 56 is connected to the gate terminal of the driving transistor 54.

The gate terminal of the switch transistor 58 is connected to a second select line SEL2. The first terminal of the switch transistor 58 is connected to a signal line VDATA. The second terminal of the switch transistor 58 is connected to the shared terminal of the storage capacitors 52 and 53 (i.e. node C2). The anode electrode of the OLED 50 is connected to a voltage supply electrode VDD.

The OLED 50 and the transistors 54 and 56 are connected at node A2. The storage capacitor 52 and the transistors 54 and 56 are connected at node B2.

FIG. 9 illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit 202 of FIG. 8. Referring to FIGS. 8 and 9, the operation of the pixel circuit 202 includes a programming cycle having four operating cycles X**21**, X**22**, X**23** and X**24**, and a driving cycle having one operating cycle X**25**.

During the programming cycle, a programming voltage plus the threshold voltage of the driving transistor **54** is stored in the storage capacitor **52**. The source terminal of the driving transistor **54** goes to zero, and the second storage capacitor **53** is charged to zero.

As a result, the gate-source voltage of the driving transistor **54** goes to:

$$VGS=VP+VT \quad (2)$$

where VGS represents the gate-source voltage of the driving transistor **54**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **54**.

In the first operating cycle X**21**: VSS goes to a high positive voltage, and VDATA is zero. SEL**1** and SEL**2** are high. Therefore, nodes A**2** and B**2** are charged to a positive voltage.

In the second operating cycle X**22**: While SEL**1** is low and the switch transistor **56** is off, VDATA goes to a high positive voltage. As a result, the voltage at node B**2** increases (i.e. bootstrapping) and node A**2** is charged to the voltage of VSS. At this voltage, the OLED **50** is off.

In the third operating cycle X**23**: VSS goes to a reference voltage VREF. VDATA goes to (VREF−VP). At the beginning of this cycle, the voltage of node B**2** becomes almost equal to the voltage of node A**2** because the capacitance **51** of the OLED **50** is bigger than that of the storage capacitor **52**. After that, the voltage of node B**2** and the voltage of node A**2** are discharged through the driving transistor **54** until the driving transistor **54** turns off. As a result, the gate-source voltage of the driving transistor **54** is (VREF+VT), and the voltage stored in storage capacitor **52** is (VP+VT).

In the fourth operating cycle X**24**: SEL**1** is low. Since SEL**2** is high, and VDATA is zero, the voltage at node C**2** goes to zero.

In the fifth operating cycle X**25**: VSS goes to its operating voltage during the driving cycle. In FIG. **5**, the operating voltage of VSS is zero. However, it may be any voltage other than zero. SEL**2** is low. The voltage stored in the storage capacitor **52** is applied to the gate terminal of the driving transistor **54**. Accordingly, a current independent of the threshold voltage VT of the driving transistor **54** and the voltage of the OLED **50** flows through the driving transistor **54** and the OLED **50**. Thus, the degradation of the OLED **50** and instability of the driving transistor **54** does not affect the amount of the current flowing through the driving transistor **54** and the OLED **50**.

FIG. **10** illustrates a pixel circuit **204** to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit **204** includes an OLED **60**, two storage capacitors **62** and **63**, a driving transistor **64**, and switch transistors **66** and **68**. The pixel circuit **204** is a top emission, voltage programmed pixel circuit. The pixel circuit **204** principally works similar to that of in FIG. **8**. However, one common select line is used to operate the pixel circuit **204**, which can increase the available pixel area and aperture ratio.

The transistors **64**, **66** and **68** are n-type TFTs. However, The transistors **64**, **66** and **68** may be p-type transistors. The driving technique applied to the pixel circuit **204** is also applicable to a complementary pixel circuit having p-type transistors as shown in FIG. **19**. The transistors **64**, **66** and **68** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

The first terminal of the driving transistor **64** is connected to the cathode electrode of the OLED **60**. The second terminal of the driving transistor **64** is connected to a controllable voltage supply line VSS. The gate terminal of the driving transistor **64** is connected to its first line (terminal) through the switch transistor **66**. The storage capacitors **62** and **63** are in series, and are connected between the gate terminal of the driving transistor **64** and the common ground. The voltage of the voltage supply line VSS is controllable. The common ground may be connected to VSS.

The gate terminal of the switch transistor **66** is connected to a select line SEL. The first terminal of the switch transistor **66** is connected to the first terminal of the driving transistor **64**. The second terminal of the switch transistor **66** is connected to the gate terminal of the driving transistor **64**.

The gate terminal of the switch transistor **68** is connected to the select line SEL. The first terminal of the switch transistor **68** is connected to a signal line VDATA. The second terminal is connected to the shared terminal of storage capacitors **62** and **63** (i.e. node C**3**). The anode electrode of the OLED **60** is connected to a voltage supply electrode VDD.

The OLED **60** and the transistors **64** and **66** are connected at node A**3**. The storage capacitor **62** and the transistors **64** and **66** are connected at node B**3**.

FIG. **11** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **204** of FIG. **10**. Referring to FIGS. **10** and **11**, the operation of the pixel circuit **204** includes a programming cycle having three operating cycles X**31**, X**32** and X**33**, and a driving cycle includes one operating cycle X**34**.

During the programming cycle, a programming voltage plus the threshold voltage of the driving transistor **64** is stored in the storage capacitor **62**. The source terminal of the driving transistor **64** goes to zero and the storage capacitor **63** is charged to zero.

As a result, the gate-source voltage of the driving transistor **64** goes to:

$$VGS=VP+VT \quad (3)$$

where VGS represents the gate-source voltage of the driving transistor **64**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **64**.

In the first operating cycle X**31**: VSS goes to a high positive voltage, and VDATA is zero. SEL is high. As a result, nodes A**3** and B**3** are charged to a positive voltage. The OLED **60** turns off.

In the second operating cycle X**32**: While SEL is high, VSS goes to a reference voltage VREF. VDATA goes to (VREF−VP). As a result, the voltage at node B**3** and the voltage of node A**3** are discharged through the driving transistor **64** until the driving transistor **64** turns off. The voltage of node B**3** is (VREF+VT), and the voltage stored in the storage capacitor **62** is (VP+VT).

In the third operating cycle X**33**: SEL goes to VM. VM is an intermediate voltage in which the switch transistor **66** is off and the switch transistor **68** is on. VDATA goes to zero. Since SEL is VM and VDATA is zero, the voltage of node C**3** goes to zero.

VM is defined as:

$$VT3 << VM < VREF+VT1+VT2 \quad (a)$$

where VT**1** represents the threshold voltage of the driving transistor **64**, VT**2** represents the threshold voltage of the switch transistor **66**, and VT**3** represents the threshold voltage of the switch transistor **68**.

The condition (a) forces the switch transistor **66** to be off and the switch transistor **68** to be on. The voltage stored in the storage capacitor **62** remains intact.

In the fourth operating cycle X**34**: VSS goes to its operating voltage during the driving cycle. In FIG. **11**, the operating voltage of VSS is zero. However, the operating voltage of VSS may be any voltage other than zero. SEL is low. The voltage stored in the storage capacitor **62** is applied to the gate of the driving transistor **64**. The driving transistor **64** is ON. Accordingly, a current independent of the threshold voltage VT of the driving transistor **64** and the voltage of the OLED **60** flows through the driving transistor **64** and the OLED **60**. Thus, the degradation of the OLED **60** and instability of the driving transistor **64** does not affect the amount of the current flowing through the driving transistor **64** and the OLED **60**.

FIG. **12** illustrates a pixel circuit **206** to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit **206** includes an OLED **70**, two storage capacitors **72** and **73**, a driving transistor **74**, and switch transistors **76** and **78**. The pixel circuit **206** is a top emission, voltage programmed pixel circuit.

The transistors **74**, **76** and **78** are n-type TFTs. However, the transistors **74**, **76** and **78** may be p-type transistors. The driving technique applied to the pixel circuit **206** is also applicable to a complementary pixel circuit having p-type transistors as shown in FIG. **21**. The transistors **74**, **76** and **78** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), NMOS/PMOS technology or CMOS technology (e.g. MOSFET).

The first terminal of the driving transistor **74** is connected to the cathode electrode of the OLED **70**. The second terminal of the driving transistor **74** is connected to a common ground. The gate terminal of the driving transistor **74** is connected to its first line (terminal) through the switch transistor **76**. The storage capacitors **72** and **73** are in series, and are connected between the gate terminal of the driving transistor **74** and the common ground.

The gate terminal of the switch transistor **76** is connected to a select line SEL. The first terminal of the switch transistor **76** is connected to the first terminal of the driving transistor **74**. The second terminal of the switch transistor **76** is connected to the gate terminal of the driving transistor **74**.

The gate terminal of the switch transistor **78** is connected to the select line SEL. The first terminal of the switch transistor **78** is connected to a signal line VDATA. The second terminal is connected to the shared terminal of storage capacitors **72** and **73** (i.e. node C**4**). The anode electrode of the OLED **70** is connected to a voltage supply electrode VDD. The voltage of the voltage electrode VDD is controllable.

The OLED **70** and the transistors **74** and **76** are connected at node A**4**. The storage capacitor **72** and the transistors **74** and **76** are connected at node B**4**.

FIG. **13** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **206** of FIG. **12**. Referring to FIGS. **12** and **13**, the operation of the pixel circuit **206** includes a programming cycle having four operating cycles X**41**, X**42**, X**43** and X**44**, and a driving cycle having one driving cycle **45**.

During the programming cycle, a programming voltage plus the threshold voltage of the driving transistor **74** is stored in the storage capacitor **72**. The source terminal of the driving transistor **74** goes to zero and the storage capacitor **73** is charged to zero.

As a result, the gate-source voltage of the driving transistor **74** goes to:

$$VGS=VP+VT \tag{4}$$

where VGS represents the gate-source voltage of the driving transistor **74**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **74**.

In the first operating cycle X**41**: SEL is high. VDATA goes to a low voltage. While VDD is high, node B**4** and node A**4** are charged to a positive voltage.

In the second operating cycle X**42**: SEL is low, and VDD goes to a reference voltage VREF where the OLED **70** is off.

In the third operating cycle X**43**: VDATA goes to (VREF**2**−VP) where VREF**2** is a reference voltage. It is assumed that VREF**2** is zero. However, VREF**2** can be any voltage other than zero. SEL is high. Therefore, the voltage of node B**4** and the voltage of node A**4** become equal at the beginning of this cycle. It is noted that the first storage capacitor **72** is large enough so that its voltage becomes dominant. After that, node B**4** is discharged through the driving transistor **74** until the driving transistor **74** turns off.

As a result, the voltage of node B**4** is VT (i.e. the threshold voltage of the driving transistor **74**). The voltage stored in the first storage capacitor **72** is (VP−VREF**2**+VT)=(VP+VT) where VREF**2**=0.

In the fourth operating cycle X**44**: SEL goes to VM where VM is an intermediate voltage at which the switch transistor **76** is off and the switch transistor **78** is on. VM satisfies the following condition:

$$VT3<<VM<VP+VT \tag{b}$$

where VT**3** represents the threshold voltage of the switch transistor **78**.

VDATA goes to VREF**2** (=0). The voltage of node C**4** goes to VREF**2** (=0).

This results in that the gate-source voltage VGS of the driving transistor **74** is (VP+VT). Since VM<VP+VT, the switch transistor **76** is off, and the voltage stored in the storage capacitor **72** stays at VP+VT.

In the fifth operating cycle X**45**: VDD goes to the operating voltage. SEL is low. The voltage stored in the storage capacitor **72** is applied to the gate of the driving transistor **74**. Accordingly, a current independent of the threshold voltage VT of the driving transistor **74** and the voltage of the OLED **70** flows through the driving transistor **74** and the OLED **70**. Thus, the degradation of the OLED **70** and instability of the driving transistor **74** does not affect the amount of the current flowing through the driving transistor **74** and the OLED **70**.

FIG. **14** illustrates a pixel circuit **208** to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit **208** includes an OLED **80**, a storage capacitor **81**, a driving transistor **84** and a switch transistor **86**. The pixel circuit **208** corresponds to the pixel circuit **200** of FIG. **3**, and a voltage programmed pixel circuit.

The transistors **84** and **86** are p-type TFTs. The transistors **84** and **86** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

The first terminal of the driving transistor **84** is connected to a controllable voltage supply line VSS. The second terminal of the driving transistor **84** is connected to the cathode electrode of the OLED **80**. The gate terminal of the driving transistor **84** is connected to a signal line VDATA through the switch transistor **86**. The storage capacitor **81** is connected between the second terminal and the gate terminal of the driving transistor **84**.

The gate terminal of the switch transistor **86** is connected to a select line SEL. The first terminal of the switch transistor **86** is connected to the signal line VDATA. The second terminal of the switch transistor **86** is connected to the gate terminal of the driving transistor **84**. The anode electrode of the OLED **80** is connected to a ground voltage supply electrode.

The storage capacitor **81** and the transistors **84** and **85** are connected at node A**5**. The OLED **80**, the storage capacitor **81** and the driving transistor **84** are connected at node B**5**.

FIG. **15** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **208** of Figure. FIG. **15** corresponds to FIG. **4**. VDATA and VSS are used to programming and compensating for a time dependent parameter of the pixel circuit **208**, which are similar to VDATA and VDD of FIG. **4**. Referring to FIGS. **14** and **15**, the operation of the pixel circuit **208** includes a programming cycle having three operating cycles X**51**, X**52** and X**53**, and a driving cycle having one operating cycle X**54**.

During the programming cycle, node B**5** is charged to a positive threshold voltage of the driving transistor **84**, and node A**5** is charged to a negative programming voltage.

As a result, the gate-source voltage of the driving transistor **84** goes to:

$$VGS=-VP+(-|VT|)=-VP-|VT| \quad (5)$$

where VGS represents the gate-source voltage of the driving transistor **84**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **84**.

In the first operating cycle X**51**: VSS goes to a positive compensating voltage VCOMPB, and VDATA goes to a negative compensating voltage (−VCOMPA), and SEL is low. As a result, the switch transistor **86** is on. Node A**5** is charged to (−VCOMPA). Node B**5** is charged to VCOMPB.

In the second operating cycle X**52**: VDATA goes to a reference voltage VREF. Node B**5** is discharged through the driving transistor **84** until the driving transistor **84** turns off. As a result, the voltage of node B**5** reaches VREF+|VT|. VSS goes to a negative voltage VL to increase the speed of this cycle X**52**. For the optimal setting time, VL is selected to be equal to the operating voltage which is the voltage of VSS during the driving cycle.

In the third operating cycle X**53**: While VSS is in the VL level, and SEL is low, node A**5** is charged to (VREF−VP). Because the capacitance **82** of the OLED **80** is large, the voltage of node B**5** stays at the positive threshold voltage of the driving transistor **84**. Therefore, the gate-source voltage of the driving transistor **84** is (−VP−|VT|), which is stored in storage capacitor **81**.

In the fourth operating cycle X**54**: SEL and VDATA go to zero. VSS goes to a high negative voltage (i.e. its operating voltage). The voltage stored in the storage capacitor **81** is applied to the gate terminal of the driving transistor **84**. Accordingly, a current independent of the voltage of the OLED **80** and the threshold voltage of the driving transistor **84** flows through the driving transistor **84** and the OLED **80**. Thus, the degradation of the OLED **80** and instability of the driving transistor **84** does not affect the amount of the current flowing through the driving transistor **84** and the OLED **80**.

It is noted that the pixel circuit **208** can be operated with different values of VCOMPB, VCOMPA, VL, VREF and VP. VCOMPB, VCOMPA, VL, VREF and VP define the lifetime of the pixel circuit. Thus, these voltages can be defined in accordance with the pixel specifications.

FIG. **16** illustrates a display system having the pixel circuit **208** of FIG. **14**. VSS**1** and VSS**2** of FIG. **16** correspond to VSS of FIG. **14**. SEL**1** and SEL**2** of FIG. **16** correspond to SEL of FIG. **14**. VDATA**1** and VDATA**2** of FIG. **16** correspond to VDATA of FIG. **14**. The array of FIG. **16** is an active matrix light emitting diode (AMOLED) display having a plurality of the pixel circuits **208** of FIG. **14**. The pixel circuits **208** are arranged in rows and columns, and interconnections **91**, **92** and **93** (VDATA**1**, SEL**2**, VSS**2**). VDATA**1** (or VDATA**2**) is shared between the common column pixels while SEL**1** (or SEL**2**) and VSS**1** (or VSS**2**) are shared between common row pixels in the array structure.

A driver **310** is provided for driving VDATA**1** and VDATA**2**. A driver **312** is provided for driving VSS**1**, VSS**2**, SEL**1** and SEL**2**. A controller **314** controls the drivers **310** and **312** to implement the programming and driving cycles described above. The timing diagram for programming and driving the display array of FIG. **6** is as shown in FIG. **2**. Each programming and driving cycle may be the same as that of FIG. **15**.

The array of FIG. **16** may have array structure shown in FIG. **7**(*a*) or **7**(*b*). The array of FIG. **16**, is produced in a manner similar to that of FIG. **6**. All of the pixel circuits including the TFTs, the storage capacitor, the SEL, VDATA, and VSS lines are fabricated together. After that, the OLEDs are fabricated for all pixel circuits. The OLED is connected to the corresponding driving transistor using a via (e.g. B**5** of FIG. **14**). The panel is finished by deposition of the top electrode on the OLEDs which can be a continuous layer, reducing the complexity of the design and can be used to turn the entire display ON/OFF or control the brightness.

FIG. **17** illustrates a pixel circuit **210** to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit **210** includes an OLED **100**, two storage capacitors **102** and **103**, a driving transistor **104**, and switch transistors **106** and **108**. The pixel circuit **210** corresponds to the pixel circuit **202** of FIG. **8**.

The transistors **104**, **106** and **108** are p-type TFTs. The transistors **84** and **86** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

In FIG. **17**, one of the terminals of the driving transistor **104** is connected to the anode electrode of the OLED **100**, while the other terminal is connected to a controllable voltage supply line VDD. The storage capacitors **102** and **103** are in series, and are connected between the gate terminal of the driving transistor **104** and a voltage supply electrode V**2**. Also, V**2** may be connected to VDD. The cathode electrode of the OLED **100** is connected to a ground voltage supply electrode.

The OLED **100** and the transistors **104** and **106** are connected at node A**6**. The storage capacitor **102** and the transistors **104** and **106** are connected at node B**6**. The transistor **108** and the storage capacitors **102** and **103** are connected at node C**6**.

FIG. **18** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **210** of FIG. **17**. FIG. **18** corresponds to FIG. **9**. VDATA and VDD are used to programming and compensating for a time dependent parameter of the pixel circuit **210**, which are similar to VDATA and VSS of FIG. **9**. Referring to FIGS. **17** and **18**, the operation of the pixel circuit **210** includes a programming cycle having four operating cycles X**61**, X**62**, X**63** and X**64**, and a driving cycle having one operating cycle X**65**.

During the programming cycle, a negative programming voltage plus the negative threshold voltage of the driving transistor **104** is stored in the storage capacitor **102**, and the second storage capacitor **103** is discharged to zero.

As a result, the gate-source voltage of the driving transistor **104** goes to:

$$VGS=-VP-|VT| \tag{6}$$

where VGS represents the gate-source voltage of the driving transistor **104**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **104**.

In the first operating cycle X**61**: VDD goes to a high negative voltage, and VDATA is set to V**2**. SEL**1** and SEL**2** are low. Therefore, nodes A**6** and B**6** are charged to a negative voltage.

In the second operating cycle X**62**: While SEL**1** is high and the switch transistor **106** is off, VDATA goes to a negative voltage. As a result, the voltage at node B**6** decreases, and the voltage of node A**6** is charged to the voltage of VDD. At this voltage, the OLED **100** is off.

In the third operating cycle X**63**: VDD goes to a reference voltage VREF. VDATA goes to (V**2**−VREF+VP) where VREF is a reference voltage. It is assumed that VREF is zero. However, VREF may be any voltage other than zero. At the beginning of this cycle, the voltage of node B**6** becomes almost equal to the voltage of node A**6** because the capacitance **101** of the OLED **100** is bigger than that of the storage capacitor **102**. After that, the voltage of node B**6** and the voltage of node A**6** are charged through the driving transistor **104** until the driving transistor **104** turns off. As a result, the gate-source voltage of the driving transistor **104** is (−VP−|VT|), which is stored in the storage capacitor **102**.

In the fourth operating cycle X**64**: SEL**1** is high. Since SEL**2** is low, and VDATA goes to V**2**, the voltage at node C**6** goes to V**2**.

In the fifth operating cycle X**65**: VDD goes to its operating voltage during the driving cycle. In FIG. **18**, the operating voltage of VDD is zero. However, the operating voltage of VDD may be any voltage. SEL**2** is high. The voltage stored in the storage capacitor **102** is applied to the gate terminal of the driving transistor **104**. Thus, a current independent of the threshold voltage VT of the driving transistor **104** and the voltage of the OLED **100** flows through the driving transistor **104** and the OLED **100**. Accordingly, the degradation of the OLED **100** and instability of the driving transistor **104** do not affect the amount of the current flowing through the driving transistor **54** and the OLED **100**.

FIG. **19** illustrates a pixel circuit **212** to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit **212** includes an OLED **110**, two storage capacitors **112** and **113**, a driving transistor **114**, and switch transistors **116** and **118**. The pixel circuit **212** corresponds to the pixel circuit **204** of FIG. **10**.

The transistors **114**, **116** and **118** are p-type TFTs. The transistors **84** and **86** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

In FIG. **19**, one of the terminals of the driving transistor **114** is connected to the anode electrode of the OLED **110**, while the other terminal is connected to a controllable voltage supply line VDD. The storage capacitors **112** and **113** are in series, and are connected between the gate terminal of the driving transistor **114** and a voltage supply electrode V**2**. Also, V**2** may be connected to VDD. The cathode electrode of the OLED **100** is connected to a ground voltage supply electrode.

The OLED **110** and the transistors **114** and **116** are connected at node A**7**. The storage capacitor **112** and the transistors **114** and **116** are connected at node B**7**. The transistor **118** and the storage capacitors **112** and **113** are connected at node C**7**.

FIG. **20** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **212** of FIG. **19**. FIG. **20** corresponds to FIG. **11**. VDATA and VDD are used to programming and compensating for a time dependent parameter of the pixel circuit **212**, which are similar to VDATA and VSS of FIG. **11**. Referring to FIGS. **19** and **20**, the operation of the pixel circuit **212** includes a programming cycle having four operating cycles X**71**, X**72** and X**73**, and a driving cycle having one operating cycle X**74**.

During the programming cycle, a negative programming voltage plus the negative threshold voltage of the driving transistor **114** is stored in the storage capacitor **112**. The storage capacitor **113** is discharged to zero.

As a result, the gate-source voltage of the driving transistor **114** goes to:

$$VGS=-VP-|VT| \tag{7}$$

where VGS represents the gate-source voltage of the driving transistor **114**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **114**.

In the first operating cycle X**71**: VDD goes to a negative voltage. SEL is low. Node A**7** and node B**7** are charged to a negative voltage.

In the second operating cycle X**72**: VDD goes to a reference voltage VREF. VDATA goes to (V**2**−VREF+VP). The voltage at node B**7** and the voltage of node A**7** are changed until the driving transistor **114** turns off. The voltage of B**7** is (−VREF−VT), and the voltage stored in the storage capacitor **112** is (−VP−|VT|).

In the third operating cycle X**73**: SEL goes to VM. VM is an intermediate voltage in which the switch transistor **106** is off and the switch transistor **118** is on. VDATA goes to V**2**. The voltage of node C**7** goes to V**2**. The voltage stored in the storage capacitor **112** is the same as that of X**72**.

In the fourth operating cycle X**74**: VDD goes to its operating voltage. SEL is high. The voltage stored in the storage capacitor **112** is applied to the gate of the driving transistor **114**. The driving transistor **114** is on. Accordingly, a current independent of the threshold voltage VT of the driving transistor **114** and the voltage of the OLED **110** flows through the driving transistor **114** and the OLED **110**.

FIG. **21** illustrates a pixel circuit **214** to which programming and driving technique in accordance with a further embodiment of the present invention is applied. The pixel circuit **214** includes an OLED **120**, two storage capacitors **122** and **123**, a driving transistor **124**, and switch transistors **126** and **128**. The pixel circuit **212** corresponds to the pixel circuit **206** of FIG. **12**.

The transistors **124**, **126** and **128** are p-type TFTs. The transistors **84** and **86** may be fabricated using amorphous silicon, nano/micro crystalline silicon, poly silicon, organic semiconductors technologies (e.g. organic TFT), CMOS technology (e.g. MOSFET) and any other technology which provides p-type transistors.

In FIG. **21**, one of the terminals of the driving transistor **124** is connected to the anode electrode of the OLED **120**, while the other terminal is connected to a voltage supply line VDD. The storage capacitors **122** and **123** are in series, and are connected between the gate terminal of the driving transistor **124** and VDD. The cathode electrode of the OLED **120** is connected to a controllable voltage supply electrode VSS.

The OLED **120** and the transistors **124** and **126** are connected at node A**8**. The storage capacitor **122** and the transistors **124** and **126** are connected at node B**8**. The transistor **128** and the storage capacitors **122** and **123** are connected at node C**8**.

FIG. **22** illustrates a timing diagram showing an example of waveforms for programming and driving the pixel circuit **214** of FIG. **21**. FIG. **22** corresponds to FIG. **13**. VDATA and VSS are used to programming and compensating for a time dependent parameter of the pixel circuit **214**, which are similar to VDATA and VDD of FIG. **13**. Referring to FIGS. **21** and **22**, the programming of the pixel circuit **214** includes a programming cycle having four operating cycles X**81**, X**82**, X**83** and X**84**, and a driving cycle having one driving cycle X**85**.

During the programming cycle, a negative programming voltage plus the negative threshold voltage of the driving transistor **124** is stored in the storage capacitor **122**. The storage capacitor **123** is discharged to zero.

As a result, the gate-source voltage of the driving transistor **124** goes to:

$$VGS=-VP-|VT| \quad (8)$$

where VGS represents the gate-source voltage of the driving transistor **114**, VP represents the programming voltage, and VT represents the threshold voltage of the driving transistor **124**.

In the first operating cycle X**81**: VDATA goes to a high voltage. SEL is low. Node A**8** and node B**8** are charged to a positive voltage.

In the second operating cycle X**82**: SEL is high. VSS goes to a reference voltage VREF**1** where the OLED **60** is off.

In the third operating cycle X**83**: VDATA goes to (VREF**2**+VP) where VREF**2** is a reference voltage. SEL is low. Therefore, the voltage of node B**8** and the voltage of node A**8** become equal at the beginning of this cycle. It is noted that the first storage capacitor **112** is large enough so that its voltage becomes dominant. After that, node B**8** is charged through the driving transistor **124** until the driving transistor **124** turns off. As a result, the voltage of node B**8** is (VDD−|VT|). The voltage stored in the first storage capacitor **122** is (−VREF**2**−VP−|VT|).

In the fourth operating cycle X**84**: SEL goes to VM where VM is an intermediate voltage at which the switch transistor **126** is off and the switch transistor **128** is on. VDATA goes to VREF**2**. The voltage of node C**8** goes to VREF**2**.

This results in that the gate-source voltage VGS of the driving transistor **124** is (−VP−|VT|). Since VM<−VP−VT, the switch transistor **126** is off, and the voltage stored in the storage capacitor **122** stays at −(VP+|VT|).

In the fifth operating cycle X**85**: VSS goes to the operating voltage. SEL is low. The voltage stored in the storage capacitor **122** is applied to the gate of the driving transistor **124**.

It is noted that a system for operating an array having the pixel circuit of FIG. **8**, **10**, **12**, **17**, **19** or **21** may be similar to that of FIG. **6** or **16**. The array having the pixel circuit of FIG. **8**, **10**, **12**, **17**, **19** or **21** may have array structure shown in FIG. **7**(*a*) or **7**(*b*).

It is noted that each transistor can be replaced with p-type or n-type transistor based on concept of complementary circuits.

According to the embodiments of the present invention, the driving transistor is in saturation regime of operation. Thus, its current is defined mainly by its gate-source voltage VGS. As a result, the current of the driving transistor remains constant even if the OLED voltage changes since its gate-source voltage is stored in the storage capacitor.

According to the embodiments of the present invention, the overdrive voltage providing to a driving transistor is generated by applying a waveform independent of the threshold voltage of the driving transistor and/or the voltage of a light emitting diode voltage.

According to the embodiments of the present invention, a stable driving technique based on bootstrapping is provided (e.g. FIGS. **2**-**12** and **16**-**20**).

The shift(s) of the characteristic(s) of a pixel element(s) (e.g. the threshold voltage shift of a driving transistor and the degradation of a light emitting device under prolonged display operation) is compensated for by voltage stored in a storage capacitor and applying it to the gate of the driving transistor. Thus, the pixel circuit can provide a stable current though the light emitting device without any effect of the shifts, which improves the display operating lifetime. Moreover, because of the circuit simplicity, it ensures higher product yield, lower fabrication cost and higher resolution than conventional pixel circuits.

All citations are hereby incorporated by reference.

The present invention has been described with regard to one or more embodiments. However, it will be apparent to persons skilled in the art that a number of variations and modifications can be made without departing from the scope of the invention as defined in the claims.

What is claimed is:

1. A display system comprising:

a pixel circuit including a drive transistor, a storage capacitor, one or more switch transistors, and a light emitting device, the drive transistor having a terminal connected to the light emitting device, the drive transistor having a threshold voltage that shifts during operation of the drive transistor;

a controllable power supply connected to a terminal of the drive transistor other than the one connected to the light emitting device for supplying the pixel circuit with a compensating voltage or with an operating voltage;

a voltage driver for supplying a programming voltage to the pixel circuit via the one or more switch transistors along a data line so as to program the pixel circuit to emit light according to display information; and

a controller configured to operate the controllable power supply, the voltage driver, and one or more select lines that control the one or more switch transistors, such that:

in response to one of the one or more select lines being activated, the compensating voltage is applied to the light emitting device, via the drive transistor, to turn off the light emitting device,

in response to applying the compensation voltage, setting the data line to a nonzero reference voltage,

responsive to setting the data line to the nonzero reference voltage, the storage capacitor is allowed to charge or discharge, through the drive transistor, until the drive transistor turns off, while the one of the one or more select lines remain activated such that the threshold voltage of the drive transistor is established across the drive transistor,

the programming voltage is applied to the pixel circuit, thereby establishing a fixed voltage across the drive transistor that accounts for instabilities in the threshold voltage of the drive transistor, and

wherein the controller is configured to operate the pixel circuit to maintain the fixed voltage across the drive transistor on the storage capacitor while turning on the operating voltage during a driving cycle of the pixel circuit, the driving cycle being separate from a programming cycle during which the fixed voltage is established on the storage capacitor.

2. The display system of claim **1**, in which the controllable power supply maintains a substantially constant pixel current as the threshold voltage of the drive transistor changes with the aging of the drive transistor.

3. The display system of claim **2**, in which the light emitting device includes an organic light emitting diode supplied with the stable pixel current from the drive transistor, and the stable pixel current maintains a substantially constant brightness of the light emitted by the organic light emitting diode.

4. The display system of claim **1**, in which the pixel circuit includes an organic light emitting diode having an operating voltage that increases as the organic light emitting diode ages.

5. The display system of claim **1**, wherein the pixel circuit is configured to receive, via a first one of the one or more switch transistors coupled to a data line, a reference voltage applied to a gate terminal of the drive transistor, while a storage capacitor coupled across the drive transistor is allowed to charge or discharge through the drive transistor until the drive transistor turns off, thereby establishing the threshold voltage of the drive transistor across the drive transistor, the reference voltage being generated on the data line by the voltage driver.

6. The display system of claim **5**, wherein the pixel circuit is further configured to receive, via the first switch transistor coupled to the data line, the programming voltage applied to the gate terminal of the drive transistor thereby establishing a fixed voltage on the storage capacitor coupled across the drive transistor, the fixed voltage being a voltage based on the threshold voltage of the drive transistor and the programming voltage.

7. The display system of claim **1**, wherein the pixel circuit is configured with the storage capacitor connected across a gate terminal of the drive transistor and the terminal of the drive transistor connected to the light emitting device, and wherein the one or more switch transistors includes a first switch transistor operated by a first select line to selectively connect the gate terminal of the drive transistor to a data line via the first switch transistor.

8. The display system of claim **1**, wherein the controller is configured to apply the compensating voltage from the controllable power supply to the light emitting device via the drive transistor so as to turn off the light emitting device during the programming cycle, the controller being further configured to adjust the controllable power supply to the operating voltage during the driving cycle.

9. The display system of claim **1**, wherein the pixel circuit is one of a plurality of pixel circuits arranged in rows and columns to form an active matrix display array, each of the plurality of pixel circuits configured to be similarly operated by the controller so as to establish a fixed voltage across the respective drive transistors of the plurality of pixel circuits that accounts for instabilities in the threshold voltages of the respective drive transistors.

10. The display system of claim **1**, wherein the light emitting device includes an organic light emitting diode and wherein at least one of the drive transistor or the one or more switch transistors is a thin film transistor.

11. The display system of claim **1**, wherein the light-emitting device is an organic light emitting diode and the drive transistor is an n-type or p-type thin film transistor.

12. A method of programming a pixel circuit that drives a current-driven light emitting device independent of a threshold voltage of a drive transistor connected in series to the light emitting device, the drive transistor being connected between the light emitting device and a controllable power supply such that the controllable power supply is not directly coupled to the light emitting device, the method comprising:

activating a select line to turn on a selection transistor coupled to a gate terminal of the drive transistor;

responsive to the activating the select line, adjusting the controllable power supply to a compensating voltage sufficient to turn off the light emitting device while the select line remains active;

responsive to the adjusting, applying a nonzero reference voltage to the drive transistor through the selection transistor while the select line remains active;

responsive to the adjusting, allowing a node of the pixel circuit to charge or discharge until the drive transistor turns off while the select line remains selected, thereby establishing the threshold voltage of the driving transistor across the drive transistor;

responsive to the drive transistor turning off, applying a programming voltage to the drive transistor, thereby establishing a fixed voltage across the drive transistor according to both the threshold voltage of the drive transistor and the applied programming voltage;

setting the controllable power supply to an operating voltage; and

deselecting the select line to complete the programming cycle and initiate a driving cycle while maintaining the fixed voltage across the drive transistor.

13. The method of claim **12**, wherein the current of the driving transistor remains constant during the driving cycle, even if the light emitting device operating voltage changes, due to the fixed voltage being stored in a storage capacitor.

14. The method of claim **12**, wherein the reference voltage is sufficient to prevent the light emitting device from being turned on prior to the initiation of the driving cycle.

15. The method of claim **12**, wherein the pixel circuit includes a storage capacitor coupled across the gate terminal and a source terminal of the drive transistor, and wherein the node of the pixel circuit allowed to charge or discharge is coupled to the source terminal of the drive transistor such that the allowing the node of the pixel circuit to charge or discharge is carried out by discharging the storage capacitor through the driving transistor until the driving transistor turns off.

16. The method of claim **12**, wherein the compensating voltage is also applied to the node of the pixel circuit allowed to charge or discharge, the method further comprising:

adjusting the controllable power supply to a high voltage during the charging or discharging of the node of the pixel circuit so as to speed up the charging or discharging.

17. The method of claim **12**, wherein the select line remains selected during the adjusting the controllable voltage supply, the allowing the node to charge or discharge, and the applying the programming voltage.

18. The method of claim **12**, wherein the pixel circuit is one of a plurality of pixel circuits arranged in rows and columns to form an active matrix display array, and wherein the method further includes the adjusting, the selecting, the allowing, and the applying for each of the plurality of pixel circuits such that a fixed voltage is established across each of the respective drive transistors according to both the threshold voltage of the respective drive transistor and the respective applied programming voltage.

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专利名称(译)	用于编程和驱动具有可控电源电压的有源矩阵发光装置像素的方法和系统		
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摘要(译)

提供了用于编程和驱动有源矩阵发光器件像素的方法和系统。像素是电压编程像素电路，并且具有发光器件，驱动晶体管和存储电容器。像素具有编程周期，该编程周期具有多个操作周期和驱动周期。在编程周期期间，控制OLED和驱动晶体管之间的连接电压，使得驱动晶体管的期望栅极 - 源极电压存储在存储电容器中。